DS26334DK/DS26324DK 3.3V, 16-Channel, E1/T1/J1 Short-/Long-Haul LIU Design Kit

www.maxim-ic.com

GENERAL DESCRIPTION

The DS26334DK/DS26324DK is a fully integrated design kit for the DS26334 and DS26324 3.3V, 16-channel, E1/T1/J1 line interface units (LIUs). This design kit contains all the necessary circuitry to evaluate the DS26334 and DS26324 in all modes of operation. The design kit also includes an on-board microprocessor to run real-time code for further part evaluation.

DESIGN KIT CONTENTS

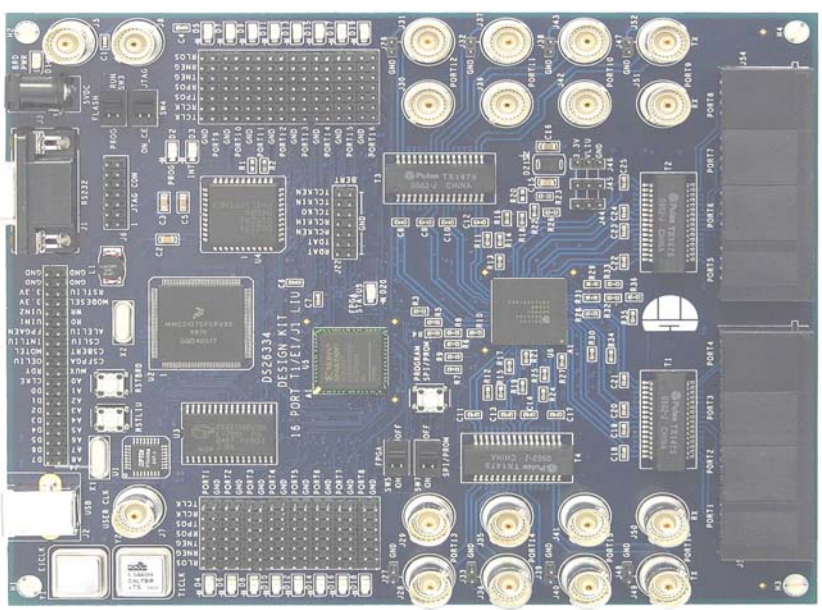
DS26334DK Board with a DS26324 or DS26334
5V AC/DC Adapter
3ft USB Cable
Download:
- ChipView Software
- DS26334DK/DS26324DK.def Definition File
- DS26334DK/DS26324DK Data Sheet

ORDERING INFORMATION

PART	DESCRIPTION
DS26334DK	Design Kit Board for DS26334
DS26324DK	Design Kit Board for DS26324

FEATURES

- **Expedites New Designs by Eliminating First-Pass Prototyping**
- **Demonstrates Key Functions of the DS26334/DS26324**
- **Includes DS26334/DS26324 x 16-Port LIU, Transformers, 75Ω BNC Connectors, RJ-48 Connectors, and Termination Passives**
- **Communicates Directly with any PC with a USB or RS-232 Serial Interface**
- **High-Level Windows®-Based Software Provides Visual Access to All Registers**
- **Software-Controlled (Register) Mapped Configuration Switches Facilitate Real-Time Clock and Signal Routing**
- **Precision Test Points for All Clocks and Signals**
- **On-Board T1 and E1 Crystal Oscillators for Stable Clock Generation**
- **On-Board BERT for Testing and Pattern Generation**



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REV: 120905

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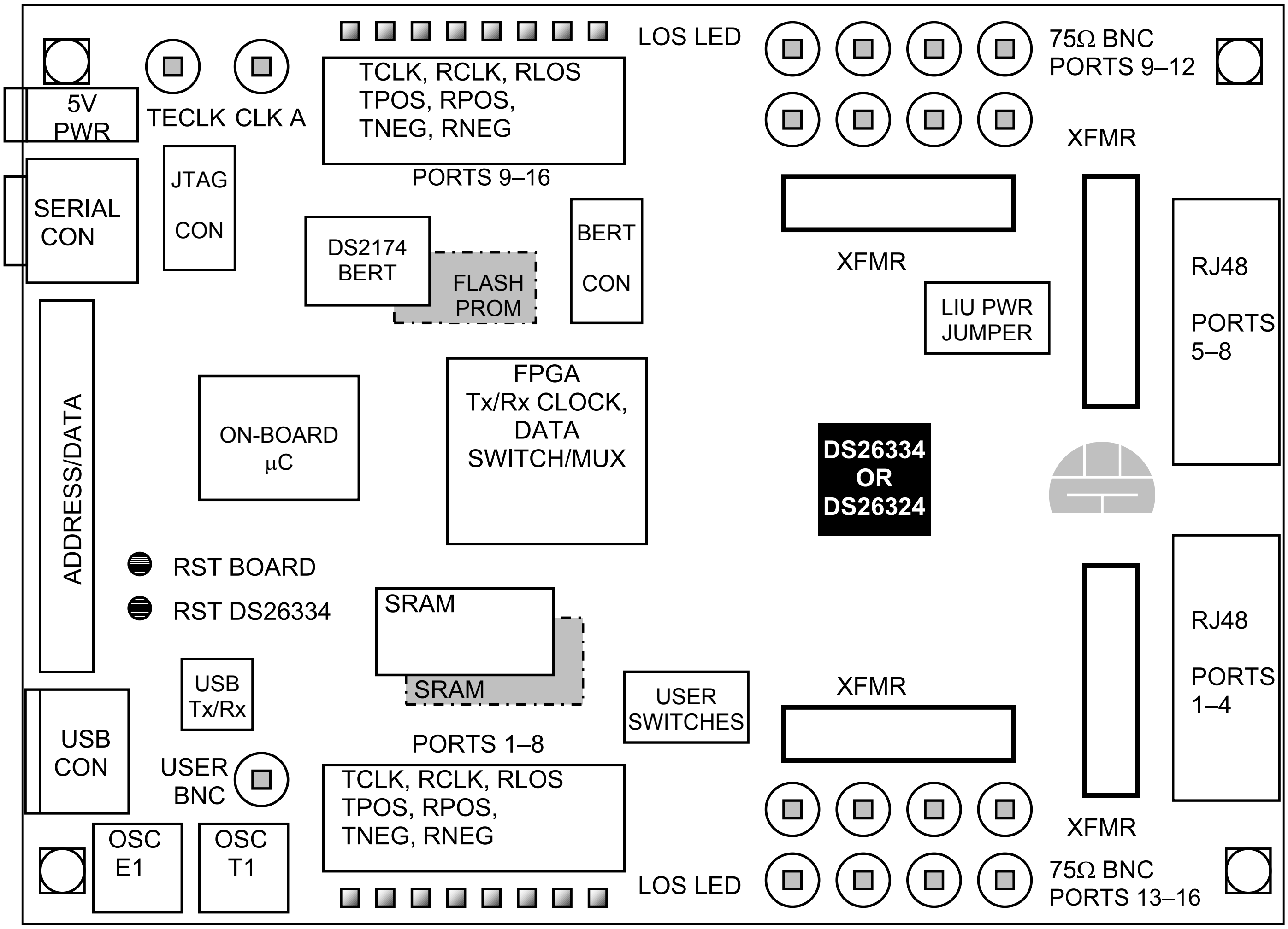
COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/ PART NUMBER
C1, C4, C6, C7, C31, C33–C41, C43–C46, C49, C51–C54, C56–C58, C61–C93, C95–C108	66	0.1µF ±20%, 16V X7R ceramic capacitors (0603)	AVX 0603YC104MAT
C2, C3, C27, C37, C42, C48, C50, C55, C59, C60	10	1µF ±10%, 16V ceramic capacitors (1206)	Panasonic ECJ-3YB1C105K
C5, C16, C26, C30, C34, C35, C94	7	10µF ±20%, 10V ceramic capacitors (1206)	Panasonic ECJ-3YB1A106M
C8–C14, C17–C25	16	470pF ±10%, 100V ceramic capacitors (0603)	Panasonic ECJ-1VB2A471K
C15	1	6.8µF ±10%, 6.3V X5R ceramic capacitors (1206)	Panasonic ECJ-3YB0J685K
C28, C29, C32, C109, C110	5	68µF ±20%, 16V tantalum capacitors (D case)	Panasonic ECS-T1CD686R
C36, C38, C47	3	22pF ±5%, 25V ceramic capacitors (0603)	AVX 06033A220JAT
C39, C40	2	10pF ±5%, 50V ceramic capacitors (1206) (tall case)	Phycomp 1206CG100J9B200
D1, D20	2	Green LEDs (SMD)	Panasonic LN1351C
D2–D19	18	Red LEDs (SMD)	Panasonic LN1251C
D21, D22, D23	3	1A, 40V Schottky diodes	International Rectifier 10BQ040
H1–H4	4	KIT, 4-40 hardware 0.75 nylon standoff and 0.25 nylon screw	Not applicable 4-40KIT2
J1	1	DB9 right-angle connector (short case)	AMP 788750-2
J2	1	Black, single right angle (Type B)	Molex Not applicable
J3	1	2.5mm connector Power jack, right-angle PC board mount	Switchcraft RAPC712
J4	1	40-pin terminal strip (dual row, vertical)	Samtec TSW-120-07-T-D
J5, J7, J8, J28–J31, J34–J37, J40–J43, J49–J52	19	5-pin, 75Ω BNC connectors (vertical)	Cambridge CP-BNCPC-004
J6, J9–J25	18	14-pin headers (dual row, vertical)	Samtec TSW-107-14-T-D
J26, J27, J32, J33, J38, J39, J47, J48	8	2-pin headers, 0.100in centers (vertical)	Samtec TSW-102-07-T-S
J44, J45, J46	3	100-mil 3-position jumpers	Samtec Not applicable
J53, J54	2	8-pin 4-port RJ45 jacks (right angle)	Molex 43223-8140
L1	1	1.0µH ±20%, 2-pin SMT inductor	Coiltronics UP1B-1R0
R1, R20, R61, R90, R138	5	Resistors (0603) **DO NOT POPULATE**	—

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/ PART NUMBER
R2, R23, R37, R38, R39, R42, R45, R47–R50, R52, R53, R55, R57–R60, R66–R69, R71, R72, R74–R76, R79, R80, R85, R88, R89, R91, R99, R103, R104, R105, R110	38	10kΩ ±5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ103V
R3–R19, R21, R22, R24–R36, R41, R44, R46, R51, R63, R64, R65, R81, R82, R102, R109, R116, R120, R121, R122, R126, R130, R131, R132, R134–R137, R139, R140, R148, R151, R153	60	33Ω ±5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ330V
R40, R70, R73, R77, R78, R83, R84, R86, R87, R92, R93, R95–R98, R100, R101, R106, R107, R108	20	330Ω ±5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ331V
R43, R62	2	15kΩ ±5%, 1/16W resistors (0603)	Panasonic ERJ-3GEYJ153V
R54	1	Resistor (1206) **DO NOT POPULATE**	—
R56	1	470Ω ±5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ471V
R94	1	51Ω ±5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ510V
R111–R115, R117, R118, R119, R123, R124, R125, R127, R128, R129, R133, R141–R144, R146, R147, R149, R150, R152, R154–R161	32	60.4Ω ±1%, 1/16W resistors (0603)	Panasonic ERJ-3EKF60R4V
R145	1	22kΩ ±5%, 1/16W resistor (0603)	Panasonic ERJ-3GEYJ223V
SW1, SW2, SW6	3	4-pin single-pole switch	Panasonic EVQPAE04M
SW3, SW4, SW5, SW7	4	6-pin slide switches (DPDT, through hole)	Tyco Electronics SSA22
T1–T4	4	32-pin transmit/receive SMT transformers (1:2 and 1:1)	Pulse Engineering TX1475
U1	1	8-bit FIFO USB UART (32-pin LQFP)	FTDI FT245BM
U2	1	MCORE Microcontroller (144-pin LQFP)	Motorola MMC2107PV
U3, U10	2	128k x 8 SRAM (32-pin SO)	Cypress CY62128VL-70SC

DESIGNATION	QTY	DESCRIPTION	SUPPLIER/ PART NUMBER
U4	1	DS2174 EBERT (44-pin PLCC, 0°C to +70°C)	Dallas Semiconductor DS2174Q
U5	1	Spartan-II 2.5V FPGA, 200k gate (256-pin BGA)	Xilinx XC2S200-5FG256C
U6	1	3.3V, 16-channel, E1/T1/J1 long-haul LIU (256-pin BGA, 0°C to +70°C)	Dallas Semiconductor DS26334
U7	1	Dual RS-232 transmitter/receiver (150-mil, 16-pin SO)	Dallas Semiconductor DS232AR
U8, U11	2	High-speed buffers	Fairchild Semiconductor NC7SZ86
U9, U20	2	1.5W, 3.3V or adj, 1A linear regulators (16-pin TSSOP-EP)	Maxim MAX1793EUE-33
U12	1	PROM for FPGA (44-pin TQFP)	Xilinx XC18V02VQ44C
U13, U14, U18	3	Hex inverters (14-pin SO)	Toshiba TC74HC04AFN
U15	1	2.5V or adj linear regulator (8-pin μMAX/SO)	Maxim MAX1792EUA25
U16	1	Platform flash in-system programmable configuration PROM (2Mb, 20-pin TSSOP)	Xilinx XCF02SVO20C
U17	1	Quad 2-input NAND gate (14-pin SO)	Toshiba TC74HC00AFN
U19	1	Switch debouncer (4-pin SOT143)	Maxim MAX6816EUS-T
X1	1	6.00MHz low-profile crystal	Pletronics LP49-26-6.00M
X2	1	8.000MHz low-profile crystal	Ecliptek Corp. EC1-8.000M
Y1	1	Oscillator, crystal clock 5V, 2.048MHz	SaRonix NTH039A-2.0480
Y2	1	Oscillator, crystal clock 5V, 1.544MHz	SaRonix NTH039A-1.5440

BOARD FLOORPLAN



BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at www.maxim-ic.com/DS26334DK.

The support files are used with an evaluation program called ChipView, which is available for download at www.maxim-ic.com/telecom.

HARDWARE CONFIGURATION

Quick Start (Hardware Settings—Single Power Supply)

- For single power-supply operation, short jumpers J44, J45, and J46 between the 3.3V pin and the VLIU pin. This connects VDD of the DS26334/DS26324 to the 3.3V supply on the design kit.
- Ensure that the FLASH switch (SW3) is in the *RUN* position.
- Ensure that the FPGA switch (SW5) is in the *ON* position.
- Ensure that the SPI/PROM switch (SW7) is in the *OFF* position.
- If using the serial port, connect an RS-232 serial cable from DS26334DK (J1) to the PC.
- If using the USB port, connect a USB cable from DS26334DK (J2) to the PC.
- Connect AC/DC adapter with an AC power source and the DS26334DK (J3). PWR LED should be on.

JTAG Configuration

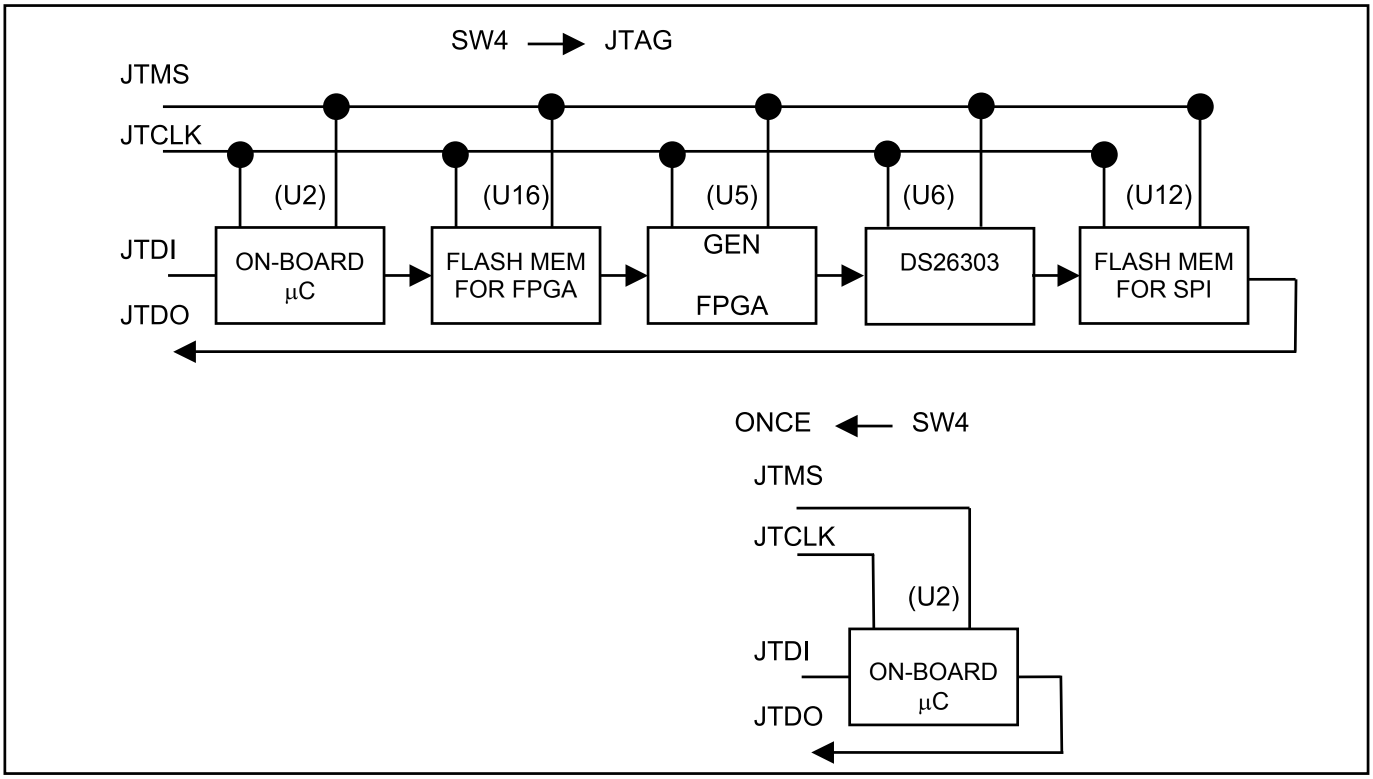
The JTAG chain is controlled by the connector JTAG CON (J6) and two on-board switches: FLASH (SW3) and ONCE/JTAG (SW4). Depending on the function, such as programming the internal microcontroller flash or performing boundary scan operations, the JTAG CON connector can be used and the switches can be configured to accomplish the desired task. For information on programming the internal flash of the on-board microcontroller, refer to the MMC2107 microcontroller user manual and board schematic.

For most purposes, having the complete JTAG chain is sufficient. Figure 1 shows the complete chain as well as what order the devices appear during boundary scan. Table 1 shows the pinout of the JTAG connector. Connect any JTAG cable to the connector to perform all operations. Note the JTAG chain changes depending on the switch SW4. The ONCE location of SW4 is used for programming the on-board microcontroller only.

Table 1. JTAG Connector (J6) Pinout

PIN	NAME
1	JTDI
2, 4, 6, 7	GND
3	JTDO
5	JTCLK
8	ALIGN KEY
9	BRD RST
10	JTMS
11	BRD V3.3
12	JDE
13	N.C.
14	JTRST

Figure 1. DS26334DK JTAG Chain



Address/Data Bus Connector

The DS26334DK has a connector (J4) to monitor all local bus activity for the design kit. All the signals can be captured with a high-impedance probe and displayed on an oscilloscope or logic analyzer. **Note:** If the FPGA switch (SW5) is in the "OFF" position, the on-board microcontroller will no longer drive any data onto the local bus. Therefore, the user can now connect the local bus of the DS26334/DS26324 into another system without making any modifications to the hardware. See Table 2 for specific pin information for connector J4.

Table 2. Address/Data Connector Pinout

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	A8	Local Address Bit 8	2	D0	Local Data Bit 0
3	A7	Local Address Bit 7	4	D1	Local Data Bit 1
5	A6	Local Address Bit 6	6	D2	Local Data Bit 2
7	A5	Local Address Bit 5	8	D3	Local Data Bit 3
9	A4	Local Address Bit 4	10	D4	Local Data Bit 4
11	A3	Local Address Bit 3	12	D5	Local Data Bit 5
13	A2	Local Address Bit 2	14	D6	Local Data Bit 6
15	A1	Local Address Bit 1	16	D7	Local Data Bit 7
17	A0	Local Address Bit 0	18	CLKE	SPI Clock Edge Select
19	MUX	Mux	20	RDY	Ready Handshake from LIU
21	CSFPGA	Chip Select FPGA	22	OE	Output Enable LIU
23	CSBERT	Chip Select DS2174	24	MOTEL	Motorola/Intel Select
25	CSLIU	Chip Select DS26334/DS26324	26	INT	Interrupt for DS26334/DS26324
27	ALELIU	Address Latch Enable	28	FPGAEN	FPGA Enable Pin
29	RD	Read Signal	30	UIN1	User Input 1
31	WR	Write Signal	32	UIN2	User Input 2
33	MODESEL	Mode Select	34, 36	3.3V	Board 3.3V
35	RSTLIU	Reset DS26334/DS26324	37–40	GND	Ground

Telecom Clock and Data Test Points

The DS26334DK has high-impedance test points for all the telecom signals that are related to the LIU. These signals are split up by port number and marked with easy to read silkscreen labels. Table 3 shows the telecom connector for port 1. The pinout for this connector is repeated for all 16 ports.

Table 3. Telecom Connector Pinout

PIN	NAME	FUNCTION
1	TCLK	Transmit Clock Input
2, 4, 6, 8, 10, 12, 14	GND	Ground
3	RCLK	Receive Clock Output
5	TPOS	Transmit Positive Data Input
7	RPOS	Receive Positive Data Output
9	TNEG	Transmit Negative Data Input
11	RNEG	Receive Positive Data Output
13	RLOS	Receive Loss-of-Signal Output

Note that the input signals in the telecom connector go from the connector to the on-board FPGA, then to the DS26334/DS26324. The FPGA was designed to perform specific signal routing functions such as looping back RPOS to TPOS on a particular port or transferring data from the on-board BERT. If you are using user-defined data and drive the signal on the connector, be sure to tri-state the input signal in the FPGA. **FAILURE TO DO SO COULD CAUSE DAMAGE TO THE FPGA**!

On-Board Bit Error-Rate Tester (BERT)

The DS26334DK has an on-board bit error-rate tester (BERT) to generate and detect errors in either pseudorandom or user-defined patterns. The BERT on the DS26334DK is the DS2174. A header for the relevant signals related to the BERT is located on the board (J22). See Table 4 for the pinout of the BERT connector. The BERT signals are routed into the FPGA and can be muxed into any of the 16 DS26334/DS26324 LIU ports under software control. For all questions concerning the operation of the on-board BERT, refer to the device data sheet available online at www.maxim-ic.com/telecom. If you are using user-defined data and driver the signal on the connector, be sure to tri-state the input signal in the FPGA. **FAILURE TO DO SO COULD CAUSE DAMAGE TO THE FPGA!**

Table 4. BERT Connector Pinout

PIN	NAME	FUNCTION
1	TCLK_EN	BERT TCLK Enable
2, 4, 6, 8, 10, 12, 14	GND	Ground
3	TCLKIN	BERT TCLK Input
5	TCLKO	BERT TCLK Output
7	RCLKIN	BERT RCLK Input
9	RCLKEN	BERT RCLK Enable
11	TDAT	BERT TDAT Output
13	RDAT	BERT RDAT Input

PROM SPI Configuration

In software mode, it is possible to configure the DS26334/DS26324 using a parallel interface or a serial peripheral interface (SPI). Most advanced microcontrollers have both a parallel interface and SPI interface such as the microcontroller on the DS26334DK. The command you send to the microcontroller through either the USB or serial port determines if that data is placed on the parallel or SPI bus. Refer to the data sheet for ChipView on the particular commands required to switch data ports.

A unique feature with the SPI port is that a PROM can be used to provide the LIU with the specific data needed for configuration. If the data in the PROM is formatted a certain way, it can seem as the PROM is acting like a controller with a SPI interface in master mode.

The most common PROMs to use for this type of application are those with an internal address accumulator. This feature for the PROM is important because the device must automatically jump to the next available address in the configuration memory. The Xilinx XC18V00 device family is a byte-wide nonvolatile memory with an autoincrement address function. The family of devices is available in 1Mb, 2Mb, and 4Mb densities. The PROM is also useful because the device can perform in-circuit programming with the JTAG port. Refer the data sheet for the XC18V00 for the JTAG codes for programming the configuration memory.

Figure 2 shows a general relationship of the timing for a SPI bus. For this case, all data is clocked into the slave device on the rising edge of SCLK. This feature can be configurable on the DS26334/DS26324.

Figure 2. SPI Timing Diagram

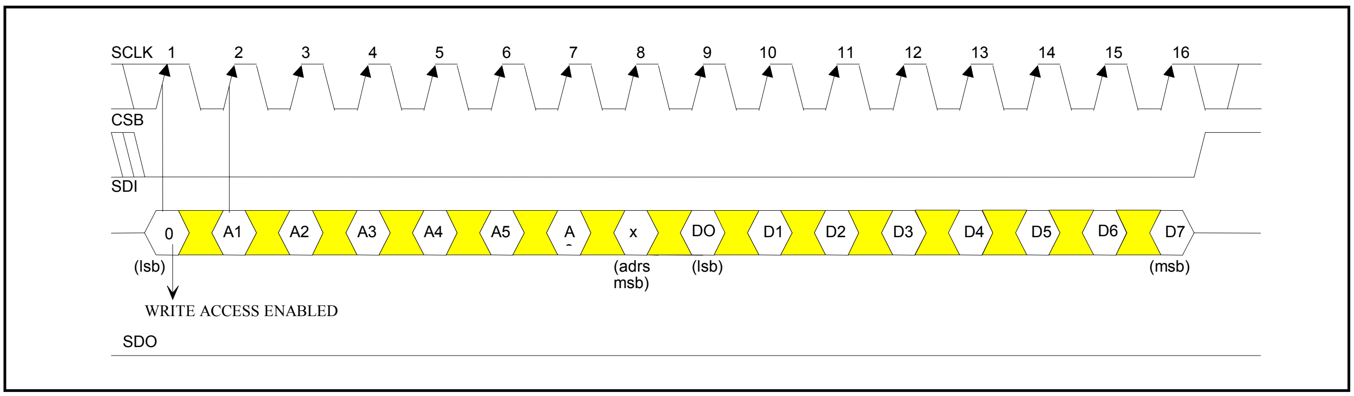


Figure 3 shows a simplified diagram of the XC18V00 device and the DS26334/DS26324 in SPI (serial) mode. Notice a few key points about this diagram. First, the CLK for the XC18V00 is the MCLK for the LIU, but this is not the SCLK for the SPI interface. The SCLK can be programmed as needed. See Table 5 for an example of the memory map. Second, the programming for this device begins when OE on the XC18V00 goes high. Therefore, consideration must be taken if some delay is necessary. Generally, it is sufficient for the OE pin to be connected to some power-up delay device. The OE delay is not necessary on this DK.

Figure 3. SPI Configuration with PROM

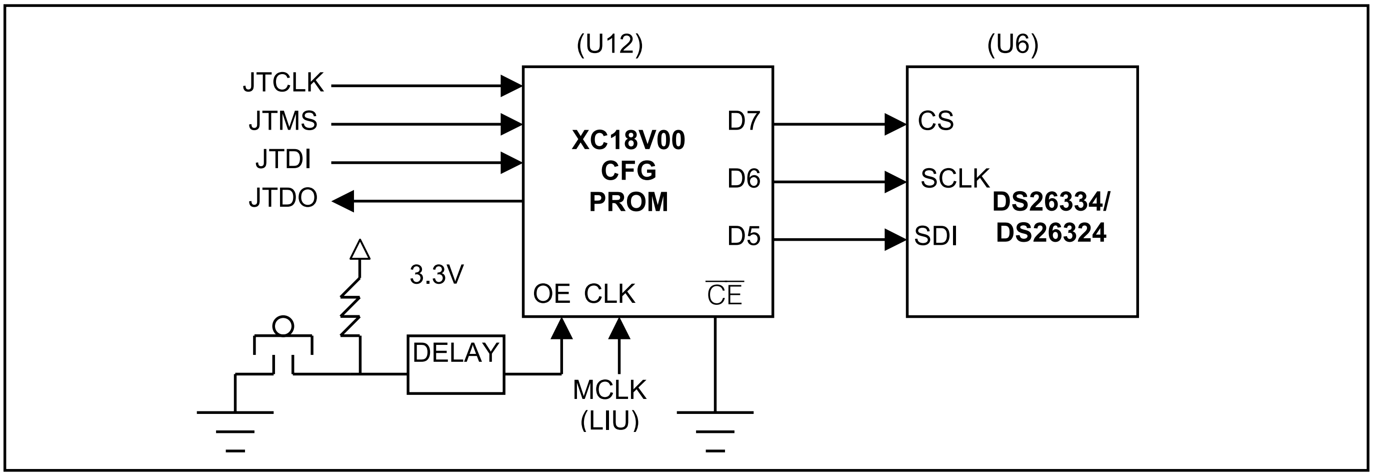


Table 5. Configuration Memory

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
	CSB	SCLK	SDI	X	X	X	X	X
0x00	1	0	0	Start of Write Cycle				
0x01	0	0	0	Bit A0 (Always a "0" for a write)				
0x02	0	1	0					
0x03	0	0	1	Bit A1				
0x04	0	1	1					
0x05	0	0	0	Bit A2				
0x06	0	1	0					
0x07	0	0	0	Bit A3				
0x08	0	1	0					
0x09	0	0	0	Bit A4				
0x0A	0	1	0					
0x0B	0	0	0	Bit A5				
0x0C	0	1	0					
0x0D	0	0	0	Bit A6				
0x0E	0	1	0					
0x0F	0	0	0	Bit A7				
0x10	0	1	0					
0x11	0	0	0	Bit D0 (LSB)				
0x12	0	1	0					
0x13	0	0	1	Bit D1				
0x14	0	1	1					
0x15	0	0	1	Bit D2				
0x16	0	1	1					
0x17	0	0	0	Bit D3				
0x18	0	1	0					
0x19	0	0	0	Bit D4				
0x1A	0	1	0					
0x1B	0	0	1	Bit D5				
0x1C	0	1	1					
0x1D	0	0	1	Bit D6				
0x1E	0	1	1					
0x1F	0	0	0	Bit D7				
0x20	0	1	0					
0x21	1	0	X	End of Write Cycle				
0x22	1	X	X					

SOFTWARE CONFIGURATION

Quick Start (Software—ChipView)

- Perform steps in the Quick Start (Hardware Configuration).
- Load ChipView software.
- Select COM port.
- Select Register View.
- From the Programs menu, launch the host application named ChipView.exe. If the default installation options were used, click the Start button on the Windows toolbar and select Programs -> ChipView -> ChipView.
- Load the DS26334DK.def file.
- Make sure that all the register settings are correct for the proper function desired for the DS26334DK.
- Refer to the DS26334 and DS26324 data sheets for all questions pertaining to device functionality.

MEMORY MAP

The on-board microcontroller is configured to start the user address space at 0x81000000. All offsets given below are relative to the beginning of the user address space.

Table 6. DS26334DK Relative Address Map

REF DES	DEVICE	OFFSET
U5	General-Purpose FPGA Tx/Rx Clock, Data Switch/Mux	0x0000
U4	DS2174 BERT	0x1000
U6	DS26334/DS26324 16-Port T1/E1/J1 LIUs	0x2000

All device registers can be easily modified using the ChipView.exe host-based user-interface software.

Table 7. General-Purpose FPGA Memory Map

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0x00	BRDID	Read-Only	Board ID
0x02	DSIDH	Read-Only	Dallas Extended ID Upper Nibble
0x03	DSIDM	Read-Only	Dallas Extended ID Middle Nibble
0x04	DSIDL	Read-Only	Dallas Extended ID Lower Nibble
0x05	BRDREV	Read-Only	Board Rev
0x06	ASMREV	Read-Only	Assembly Rev
0x07	FPGAREV	Read-Only	FPGA Firmware Rev
0x08	CTRL1	Control	Control Register 1
0x0A	ABSP	Control	Address Bank Select Pointer
0x0B	BTCLK	Control	BERT TCLK Input
0x0C	BRCLK	Control	BERT RCLK Input
0x0D	BRDAT	Control	BERT RDAT Input
0x10	TCLK	Control	Indirect Register for TCLK Source Control
0x11	TPOS	Control	Indirect Register for TPOS Source Control
0x12	TNEG	Control	Indirect Register for TPOS Source Control

ID REGISTERS

BID: BOARD ID (Offset = 0X0000)

BID is read-only with a value of 0xD.

XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0X0002)

XBIDH is read-only with a value of 0x0.

XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0X0003)

XBIDM is read-only with a value of 0x1.

XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0X0004)

XBIDL is read-only with a value of 0x6.

BREV: BOARD FAB REVISION (Offset = 0X0005)

BREV is read-only and displays the current fab revision.

AREV: BOARD ASSEMBLY REVISION (Offset = 0X0006)

AREV is read-only and displays the current assembly revision.

PREV: FPGA REVISION (Offset = 0X0007)

PREV is read-only and displays the current PLD firmware revision.

CONTROL REGISTERS

Register Name: **CTRL_1**
Register Description: **DS26334DK FPGA CONTROL REGISTER 1**
Register Offset: **0x08**

Bit #	7	6	5	4	3	2	1	0
Name	ENRLOS16	ENRLOS15	CLKE	SPI_SWAP	SPI	OE	MCLK1	MCLK0

Bit 7: ENRLOS16. This bit enables the RLOS16 LED. This should not be enabled when driving TECLK from the DS26334/DS26324.

If ENRLOS16 = LOW, the RLOS16 LED is not enabled.
If ENRLOS16 = HIGH, the RLOS16 LED is enabled and lights when RLOS16 is high.

Bit 6: ENRLOS15. This bit enables the RLOS15 LED. This should not be enabled when driving CLKA from the DS26334/DS26324.

If ENRLOS15 = LOW, the RLOS15 LED is not enabled.
If ENRLOS15 = HIGH, the RLOS15 LED is enabled and lights when RLOS15 is high.

Bit 5: CLKE. This bit sets the CLKE pin on the DS26334/DS26324. This is only active when SPI (Bit 0) is HIGH. If SPI (Bit 0) is low, CLKE is always low.

If CLKE = LOW, SDO is clocked out on the rising edge of SCLK.
If CLKE = HIGH, SDO is clocked out on the falling edge of SCLK.

Bit 4: SPI_SWAP. This bit sets the BSWP/A5 pin on the DS26334/DS26324. This is only active when SPI (Bit 0) is HIGH.

If SPI_SWAP = LOW, the SPI bus is LSB first.
If SPI_SWAP = HIGH, the SPI bus is MSB first.

Bit 3: SPI. This bit sets up the FPGA to use serial mode. This bit also changes the mode pin on the DS26334/DS26324.

If SPI = LOW, the parallel bus is used for all read/write access. This also sets the MODE pin on the DS26334/DS26324 to logic 1.
If SPI = HIGH, the SPI bus is used for all read/write access. This also sets the MODE pin on the DS26334/DS26324 to logic 0.

Bit 2: OE. This bit controls the OE pin to the DS26334.

Bits 1 and 0: MCLK1 and MCLK0. These bits control the MCLK pin to the DS26334/DS26324.

MCLK1	MCLK0	DESCRIPTION OF MCLK
0	0	MCLK = high-impedance mode
0	1	MCLK = on-board T1 oscillator
1	0	MCLK = on-board E1 oscillator
1	1	MCLK = user clock input

Register Name: **ABSP**
Register Description: **ADDRESS BANK SWAP POINTER**
Register Offset: **0x0A**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bits 7 to 0: D7 to D0. These bits control the address bank for address 0x10 (TCLK N), 0x11 (TPOS), and 0x12 (TNEG).

ABSP	DESCRIPTION
0x00	Bank Address Value for Port 1
0x01	Bank Address Value for Port 2
0x02	Bank Address Value for Port 3
0x03	Bank Address Value for Port 4
0x04	Bank Address Value for Port 5
0x05	Bank Address Value for Port 6
0x06	Bank Address Value for Port 7
0x07	Bank Address Value for Port 8
0x08	Bank Address Value for Port 9
0x09	Bank Address Value for Port 10
0x0A	Bank Address Value for Port 11
0x0B	Bank Address Value for Port 12
0x0C	Bank Address Value for Port 13
0x0D	Bank Address Value for Port 14
0x0E	Bank Address Value for Port 15
0x0F	Bank Address Value for Port 16

Register Name: **BTCLK**
Register Description: **BERT TCLK SOURCE**
Register Offset: **0x0B**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bits 7 to 0: D7 to D0. These bits control the source of the TCLK for the BERT.

BTCLK	DESCRIPTION
0x00	RCLK Port 1
0x01	RCLK Port 2
0x02	RCLK Port 3
0x03	RCLK Port 4
0x04	RCLK Port 5
0x05	RCLK Port 6
0x06	RCLK Port 7
0x07	RCLK Port 8
0x08	RCLK Port 9
0x09	RCLK Port 10
0x0A	RCLK Port 11
0x0B	RCLK Port 12
0x0C	RCLK Port 13
0x0D	RCLK Port 14
0x0E	RCLK Port 15
0x0F	RCLK Port 16
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26334
0x14	TECLK DS26334
0x15	TCLKBERT OUT
0x16–0xFF	HI-Z

Register Name: **BRCLK**
Register Description: **BERT RCLK SOURCE**
Register Offset: **0x0C**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bits 7 to 0: D7 to D0. These bits control the source of the RCLK for the BERT.

BTCLK	DESCRIPTION
0x00	RCLK Port 1
0x01	RCLK Port 2
0x02	RCLK Port 3
0x03	RCLK Port 4
0x04	RCLK Port 5
0x05	RCLK Port 6
0x06	RCLK Port 7
0x07	RCLK Port 8
0x08	RCLK Port 9
0x09	RCLK Port 10
0x0A	RCLK Port 11
0x0B	RCLK Port 12
0x0C	RCLK Port 13
0x0D	RCLK Port 14
0x0E	RCLK Port 15
0x0F	RCLK Port 16
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26334/DS26324
0x14	TECLK DS26334/DS26324
0x15	TCLKBERT OUT
0x16–0xFF	HI-Z

Register Name: **BRDAT**
Register Description: **BERT RDAT SOURCE**
Register Offset: **0x0D**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bits 7 to 0: D7 to D0. These bits control the source of the RDAT for the BERT. Note that the DS26334/DS26324 must be in single-rail mode for BERT to function properly.

BRDAT	DESCRIPTION
0x00	RPOS Port 1
0x01	RPOS Port 2
0x02	RPOS Port 3
0x03	RPOS Port 4
0x04	RPOS Port 5
0x05	RPOS Port 6
0x06	RPOS Port 7
0x07	RPOS Port 8
0x08	RPOS Port 9
0x09	RPOS Port 10
0x0A	RPOS Port 11
0x0B	RPOS Port 12
0x0C	RPOS Port 13
0x0D	RPOS Port 14
0x0E	RPOS Port 15
0x0F	RPOS Port 16
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26334/DS26324
0x14	TECLK DS26334/DS26324
0x15	TCLKBERT OUT
0x16–0xFF	HI-Z

Register Name: **TCLK**
Register Description: **PORT TCLK SOURCE**
Register Offset: **0x10**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Note: *This is an indirect register that is related to ABSP (0x0A). See register description.*

Bits 7 to 0: D7 to D0. These bits control the source of the port TCLK for the DS26334/DS26324.

TCLK	DESCRIPTION
0x00	RCLK Port 1
0x01	RCLK Port 2
0x02	RCLK Port 3
0x03	RCLK Port 4
0x04	RCLK Port 5
0x05	RCLK Port 6
0x06	RCLK Port 7
0x07	RCLK Port 8
0x08	RCLK Port 9
0x09	RCLK Port 10
0x0A	RCLK Port 11
0x0B	RCLK Port 12
0x0C	RCLK Port 13
0x0D	RCLK Port 14
0x0E	RCLK Port 15
0x0F	RCLK Port 16
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26334/DS26324
0x14	TECLK DS26334/DS26324
0x15	TCLKBERT OUT
0x16–0xFF	HI-Z

Register Name: **TPOS**
Register Description: **PORT TPOS SOURCE**
Register Offset: **0x11**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Note: *This is an indirect register that is related to ABSP (0x0A). See register description.*

Bits 7 to 0: D7 to D0. These bits control the source of the port TPOS for the DS26334/DS26324.

TPOS	DESCRIPTION
0x00	RPOS Port 1
0x01	RPOS Port 2
0x02	RPOS Port 3
0x03	RPOS Port 4
0x04	RPOS Port 5
0x05	RPOS Port 6
0x06	RPOS Port 7
0x07	RPOS Port 8
0x08	RPOS Port 9
0x09	RPOS Port 10
0x0A	RPOS Port 11
0x0B	RPOS Port 12
0x0C	RPOS Port 13
0x0D	RPOS Port 14
0x0E	RPOS Port 15
0x0F	RPOS Port 16
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26334/DS26324
0x14	TECLK DS26334/DS26324
0x15	TDATBERT OUT
0x16–0xFF	HI-Z

Register Name: **TNEG**
Register Description: **PORT TNEG SOURCE**
Register Offset: **0x12**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Note: *This is an indirect register that is related to ABSP (0x0A). See register description.*

Bits 7 to 0: D7 to D0. These bits control the source of the port TNEG for the DS26334/DS26324.

TNEG	DESCRIPTION
0x00	RNEG Port 1
0x01	RNEG Port 2
0x02	RNEG Port 3
0x03	RNEG Port 4
0x04	RNEG Port 5
0x05	RNEG Port 6
0x06	RNEG Port 7
0x07	RNEG Port 8
0x08	RNEG Port 9
0x09	RNEG Port 10
0x0A	RNEG Port 11
0x0B	RNEG Port 12
0x0C	RNEG Port 13
0x0D	RNEG Port 14
0x0E	RNEG Port 15
0x0F	RNEG Port 16
0x10	1.544MHz On-board oscillator
0x11	2.048MHz On-board oscillator
0x12	User clock
0x13	CLKA DS26334/DS26324
0x14	TECLK DS26334/DS26324
0x15	Drive Logic “0”
0x16-0xFF	HI-Z

DS26334 INFORMATION

For more information about the DS26334, refer to the DS26334 data sheet available on our website at www.maxim-ic.com/DS26334.

DS26324 INFORMATION

For more information about the DS26324, refer to the DS26324 data sheet available on our website at www.maxim-ic.com/DS26324.

DS26334DK/DS26324DK INFORMATION

For more information about the DS26334DK/DS26324DK including software downloads, go to www.maxim-ic.com/DS26334DK.

TECHNICAL SUPPORT

For additional technical support, go to www.maxim-ic.com/support.

ERRATA

On page 18 of the schematic, EB0 and EB1 were swapped in the design on U3 and U10, respectively. These changes have been made to the board using jumper wires.

SCHEMATICS

The DS26334DK/DS26324DK schematics are featured in the following 25 pages.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

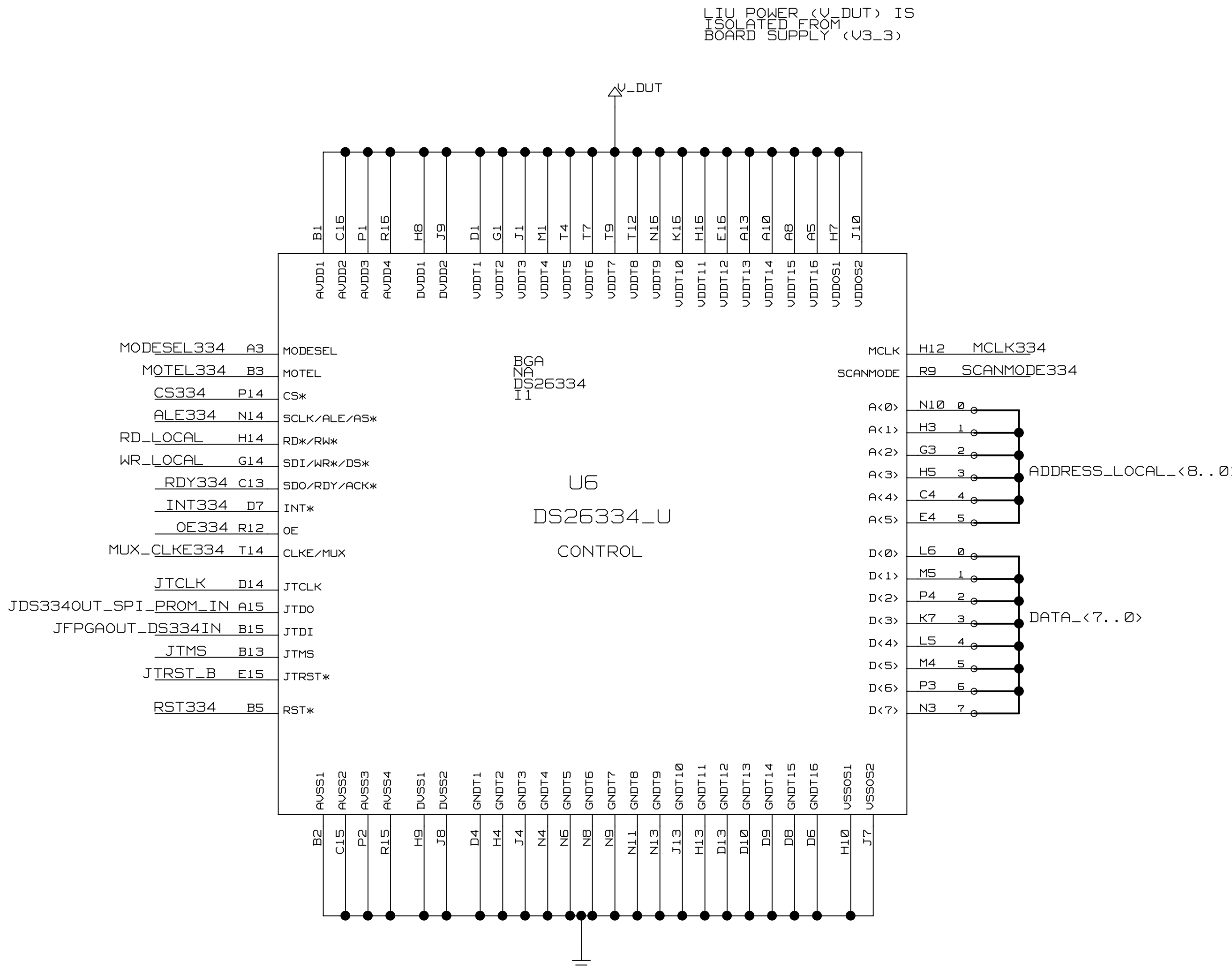
DS26334 DESIGN KIT
SCHEMATIC

DALLAS SEMICONDUCTOR / MAXIM

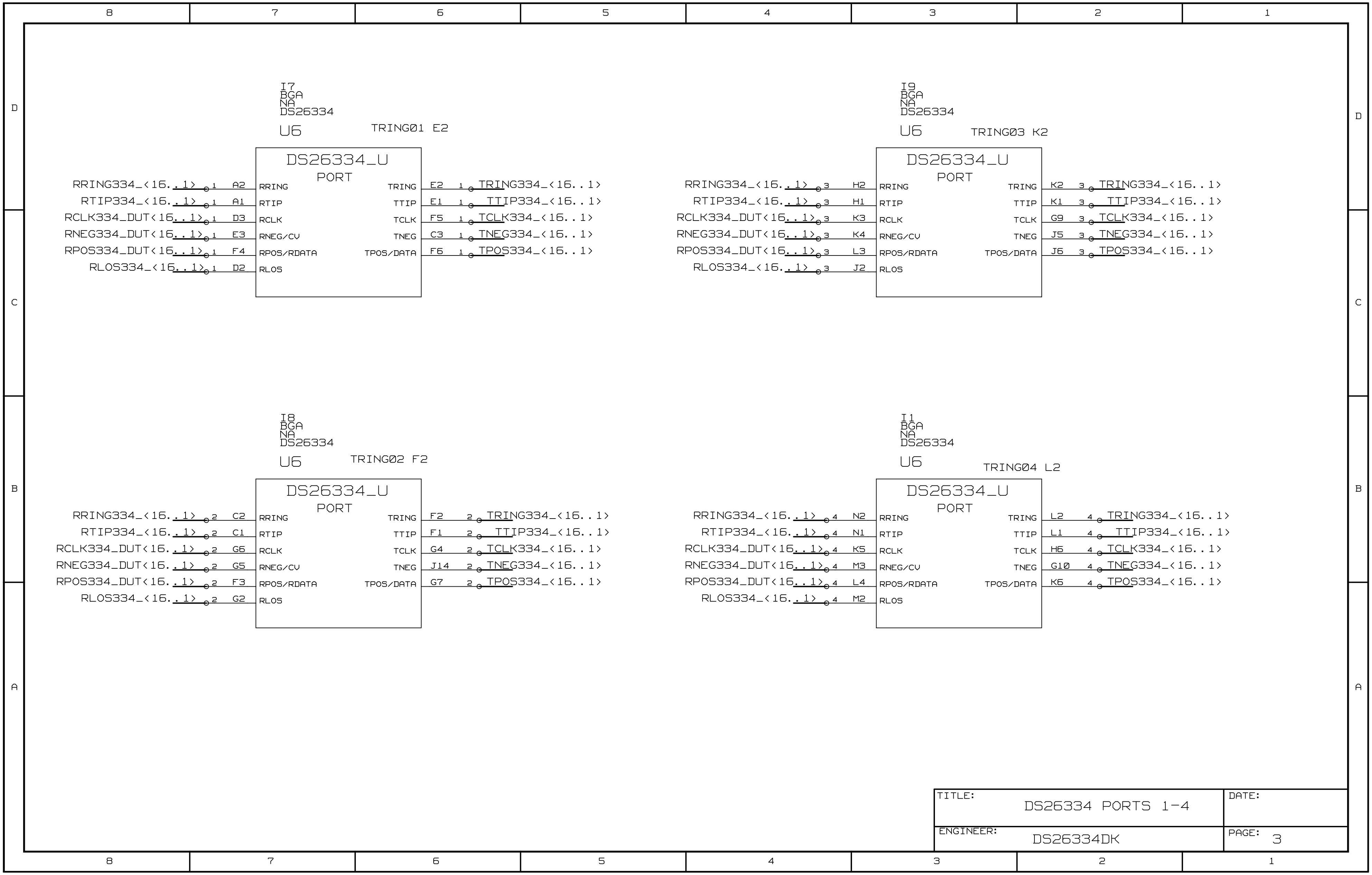
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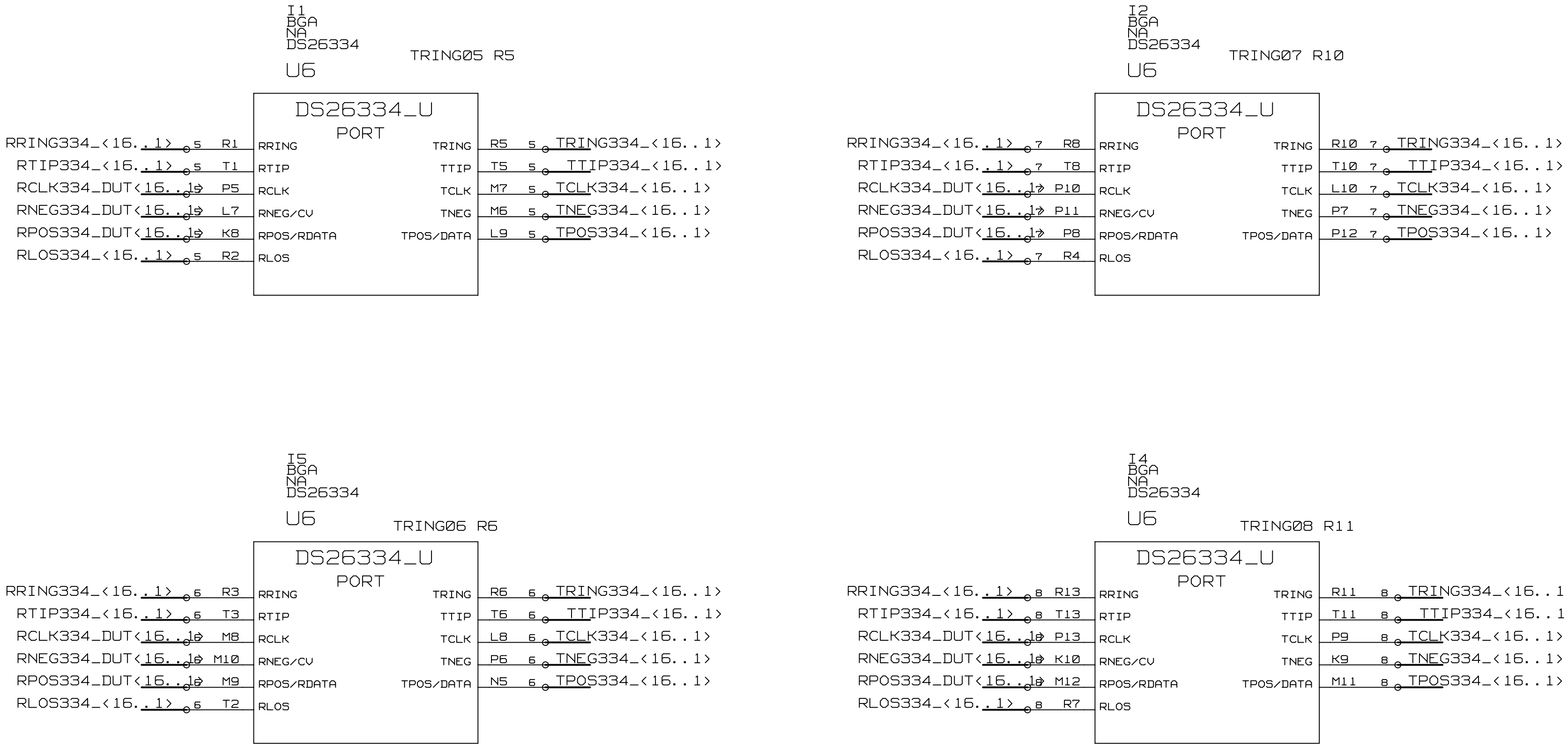
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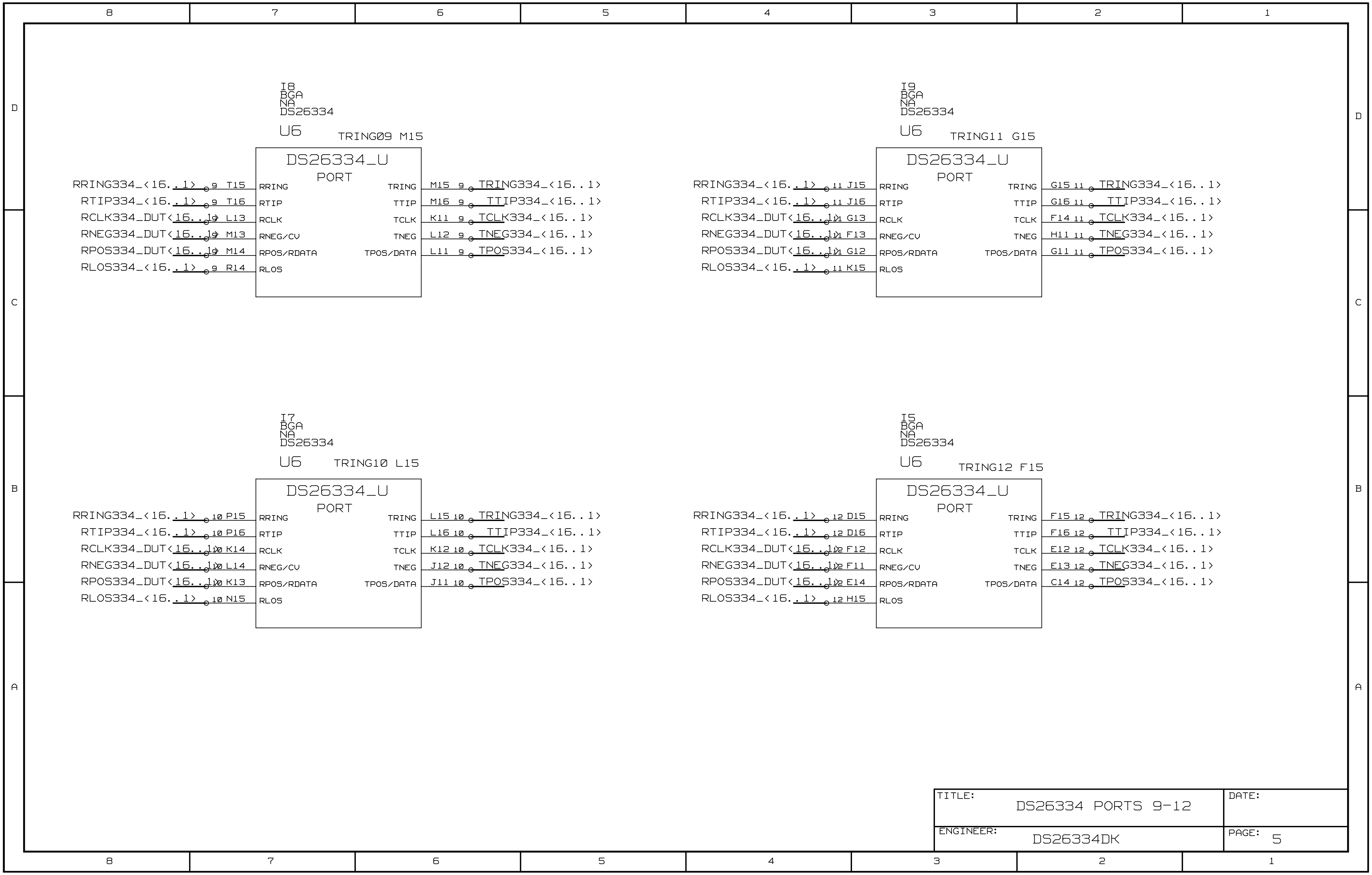


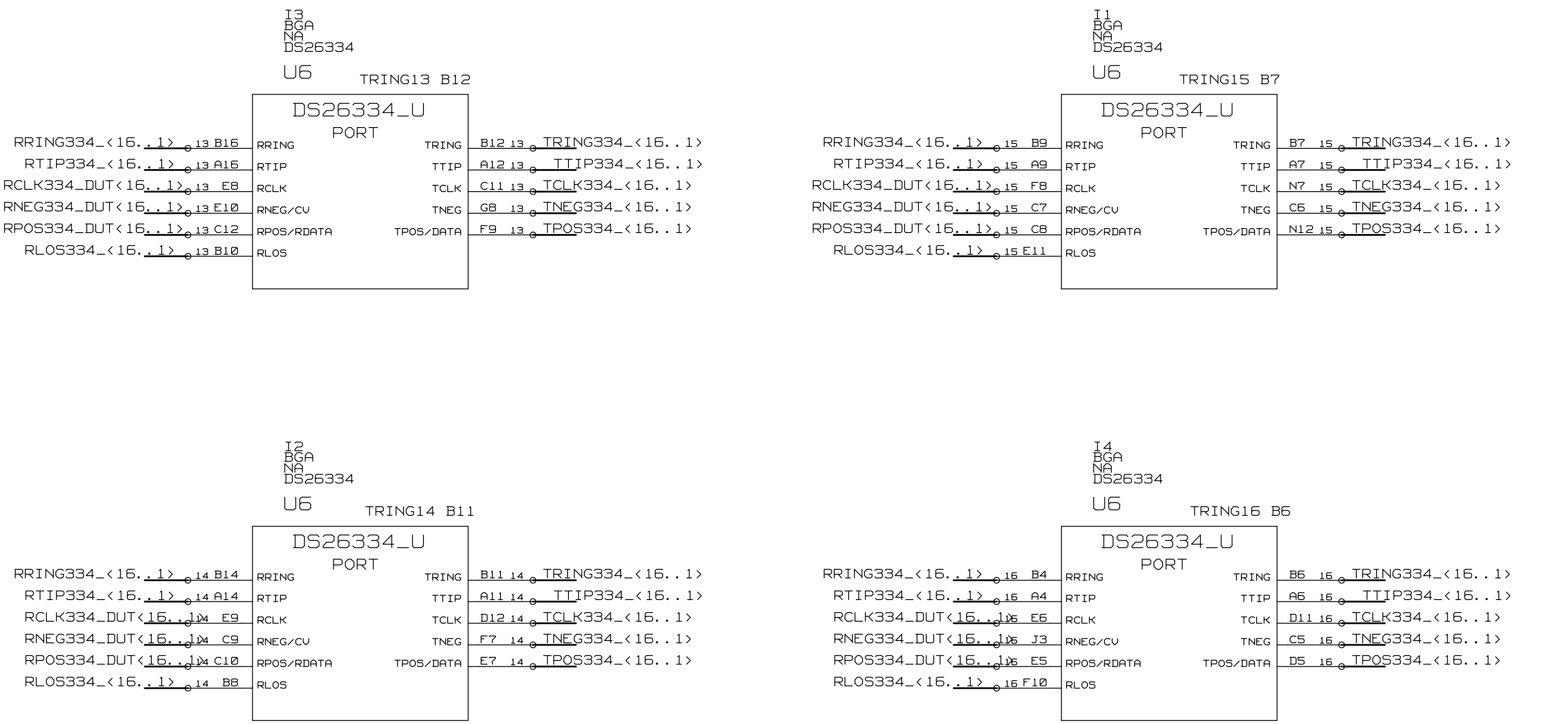
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I7 BGA NA DS26334
U6
TRING01 E2
DS26334_U
PORT
RRING334_<16..1> 1 A2 RRING
RTIP334_<16..1> 1 A1 RTIP
RCLK334_DUT<16..1> 1 D3 RCLK
RNEG334_DUT<16..1> 1 E3 RNEG/CV
RPOS334_DUT<16..1> 1 F4 RPOS/RDATA
RLOS334_<16..1> 1 D2 RLOS
TRING E2 1 TRING334_<16..1>
TTIP E1 1 TTIP334_<16..1>
TCLK F5 1 TCLK334_<16..1>
TNEG C3 1 TNEG334_<16..1>
TPOS/DATA F6 1 TPOS334_<16..1>
I9 BGA NA DS26334
U6
TRING03 K2
DS26334_U
PORT
RRING334_<16..1> 3 H2 RRING
RTIP334_<16..1> 3 H1 RTIP
RCLK334_DUT<16..1> 3 K3 RCLK
RNEG334_DUT<16..1> 3 K4 RNEG/CV
RPOS334_DUT<16..1> 3 L3 RPOS/RDATA
RLOS334_<16..1> 3 J2 RLOS
TRING K2 3 TRING334_<16..1>
TTIP K1 3 TTIP334_<16..1>
TCLK G9 3 TCLK334_<16..1>
TNEG J5 3 TNEG334_<16..1>
TPOS/DATA J6 3 TPOS334_<16..1>
I8 BGA NA DS26334
U6
TRING02 F2
DS26334_U
PORT
RRING334_<16..1> 2 C2 RRING
RTIP334_<16..1> 2 C1 RTIP
RCLK334_DUT<16..1> 2 G6 RCLK
RNEG334_DUT<16..1> 2 G5 RNEG/CV
RPOS334_DUT<16..1> 2 F3 RPOS/RDATA
RLOS334_<16..1> 2 G2 RLOS
TRING F2 2 TRING334_<16..1>
TTIP F1 2 TTIP334_<16..1>
TCLK G4 2 TCLK334_<16..1>
TNEG J14 2 TNEG334_<16..1>
TPOS/DATA G7 2 TPOS334_<16..1>
I1 BGA NA DS26334
U6
TRING04 L2
DS26334_U
PORT
RRING334_<16..1> 4 N2 RRING
RTIP334_<16..1> 4 N1 RTIP
RCLK334_DUT<16..1> 4 K5 RCLK
RNEG334_DUT<16..1> 4 M3 RNEG/CV
RPOS334_DUT<16..1> 4 L4 RPOS/RDATA
RLOS334_<16..1> 4 M2 RLOS
TRING L2 4 TRING334_<16..1>
TTIP L1 4 TTIP334_<16..1>
TCLK H6 4 TCLK334_<16..1>
TNEG G10 4 TNEG334_<16..1>
TPOS/DATA K6 4 TPOS334_<16..1>
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I8
BGA
NA
DS26334
U6
TRING09 M15
DS26334_U
PORT
RRING334_<16..1> 9 T15 RRING
RTIP334_<16..1> 9 T16 RTIP
RCLK334_DUT<16..1> 9 L13 RCLK
RNEG334_DUT<16..1> 9 M13 RNEG/CV
RPOS334_DUT<16..1> 9 M14 RPOS/RDATA
RLOS334_<16..1> 9 R14 RLOS
TRING M15 9 TRING334_<16..1>
TTIP M16 9 TTIP334_<16..1>
TCLK K11 9 TCLK334_<16..1>
TNEG L12 9 TNEG334_<16..1>
TPOS/DATA L11 9 TPOS334_<16..1>
I9
BGA
NA
DS26334
U6
TRING11 G15
DS26334_U
PORT
RRING334_<16..1> 11 J15 RRING
RTIP334_<16..1> 11 J16 RTIP
RCLK334_DUT<16..1> 11 G13 RCLK
RNEG334_DUT<16..1> 11 F13 RNEG/CV
RPOS334_DUT<16..1> 11 G12 RPOS/RDATA
RLOS334_<16..1> 11 K15 RLOS
TRING G15 11 TRING334_<16..1>
TTIP G16 11 TTIP334_<16..1>
TCLK F14 11 TCLK334_<16..1>
TNEG H11 11 TNEG334_<16..1>
TPOS/DATA G11 11 TPOS334_<16..1>
I7
BGA
NA
DS26334
U6
TRING10 L15
DS26334_U
PORT
RRING334_<16..1> 10 P15 RRING
RTIP334_<16..1> 10 P16 RTIP
RCLK334_DUT<16..1> 10 K14 RCLK
RNEG334_DUT<16..1> 10 L14 RNEG/CV
RPOS334_DUT<16..1> 10 K13 RPOS/RDATA
RLOS334_<16..1> 10 N15 RLOS
TRING L15 10 TRING334_<16..1>
TTIP L16 10 TTIP334_<16..1>
TCLK K12 10 TCLK334_<16..1>
TNEG J12 10 TNEG334_<16..1>
TPOS/DATA J11 10 TPOS334_<16..1>
I5
BGA
NA
DS26334
U6
TRING12 F15
DS26334_U
PORT
RRING334_<16..1> 12 D15 RRING
RTIP334_<16..1> 12 D16 RTIP
RCLK334_DUT<16..1> 12 F12 RCLK
RNEG334_DUT<16..1> 12 F11 RNEG/CV
RPOS334_DUT<16..1> 12 E14 RPOS/RDATA
RLOS334_<16..1> 12 H15 RLOS
TRING F15 12 TRING334_<16..1>
TTIP F16 12 TTIP334_<16..1>
TCLK E12 12 TCLK334_<16..1>
TNEG E13 12 TNEG334_<16..1>
TPOS/DATA C14 12 TPOS334_<16..1>
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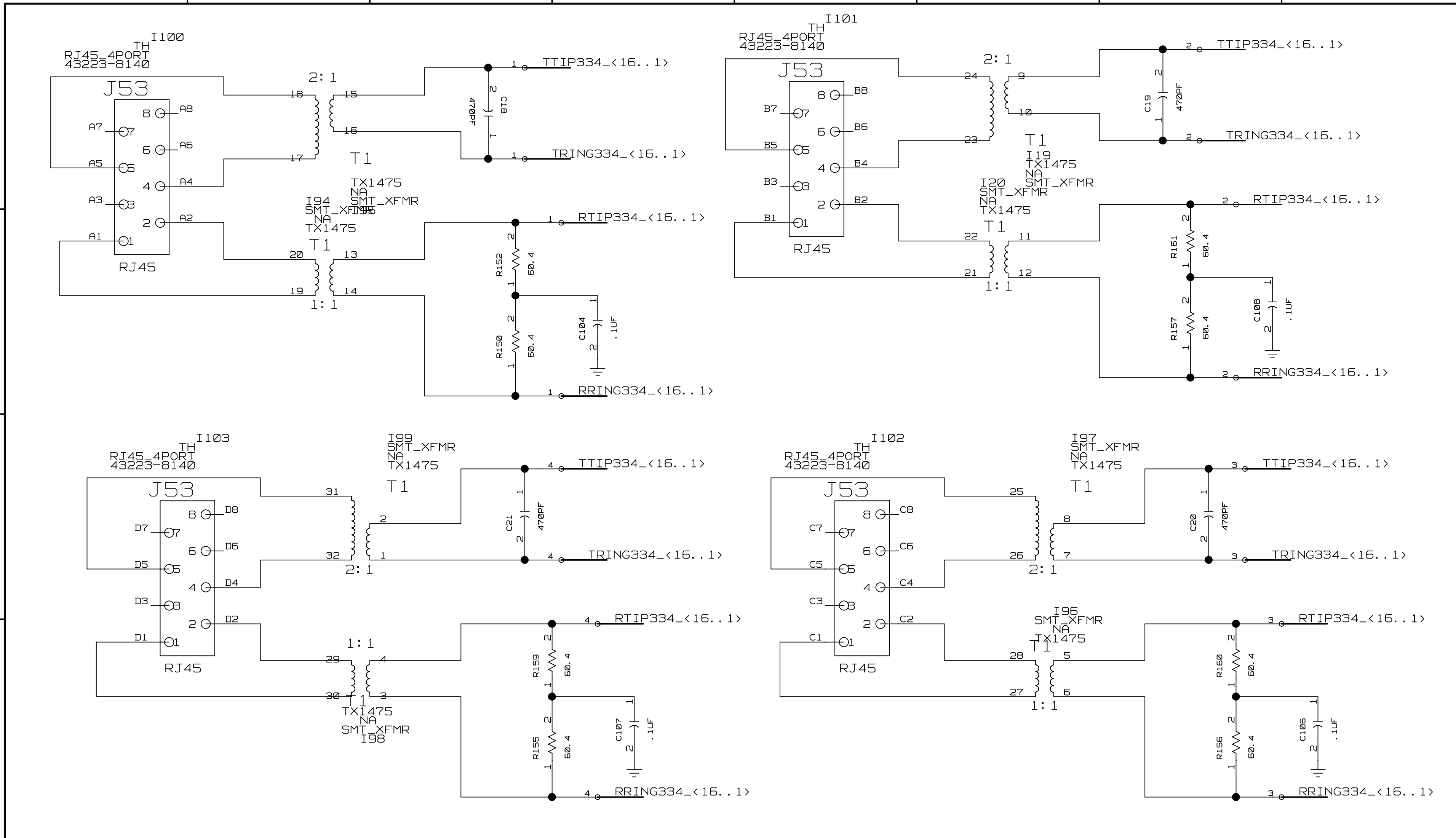


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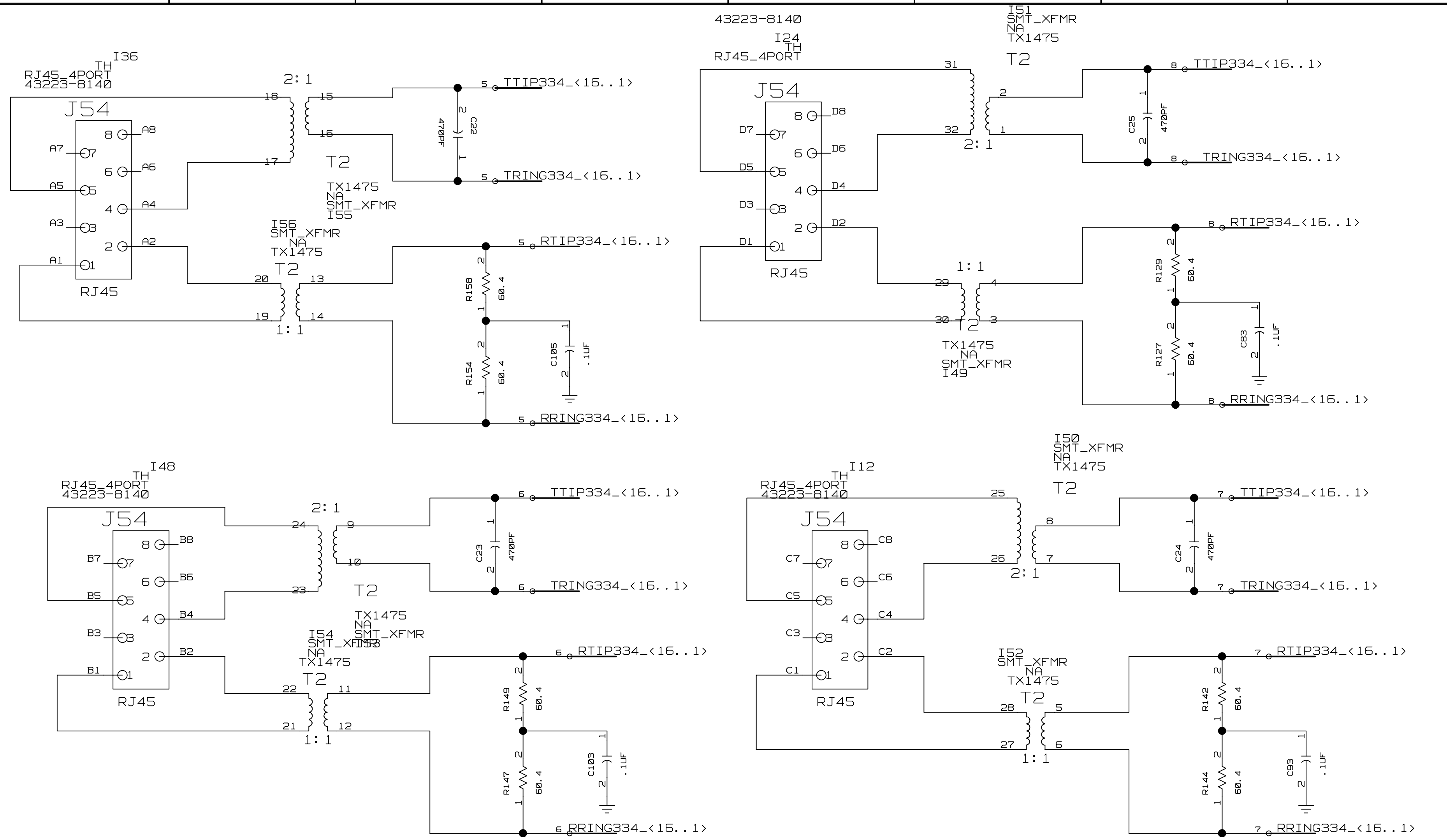
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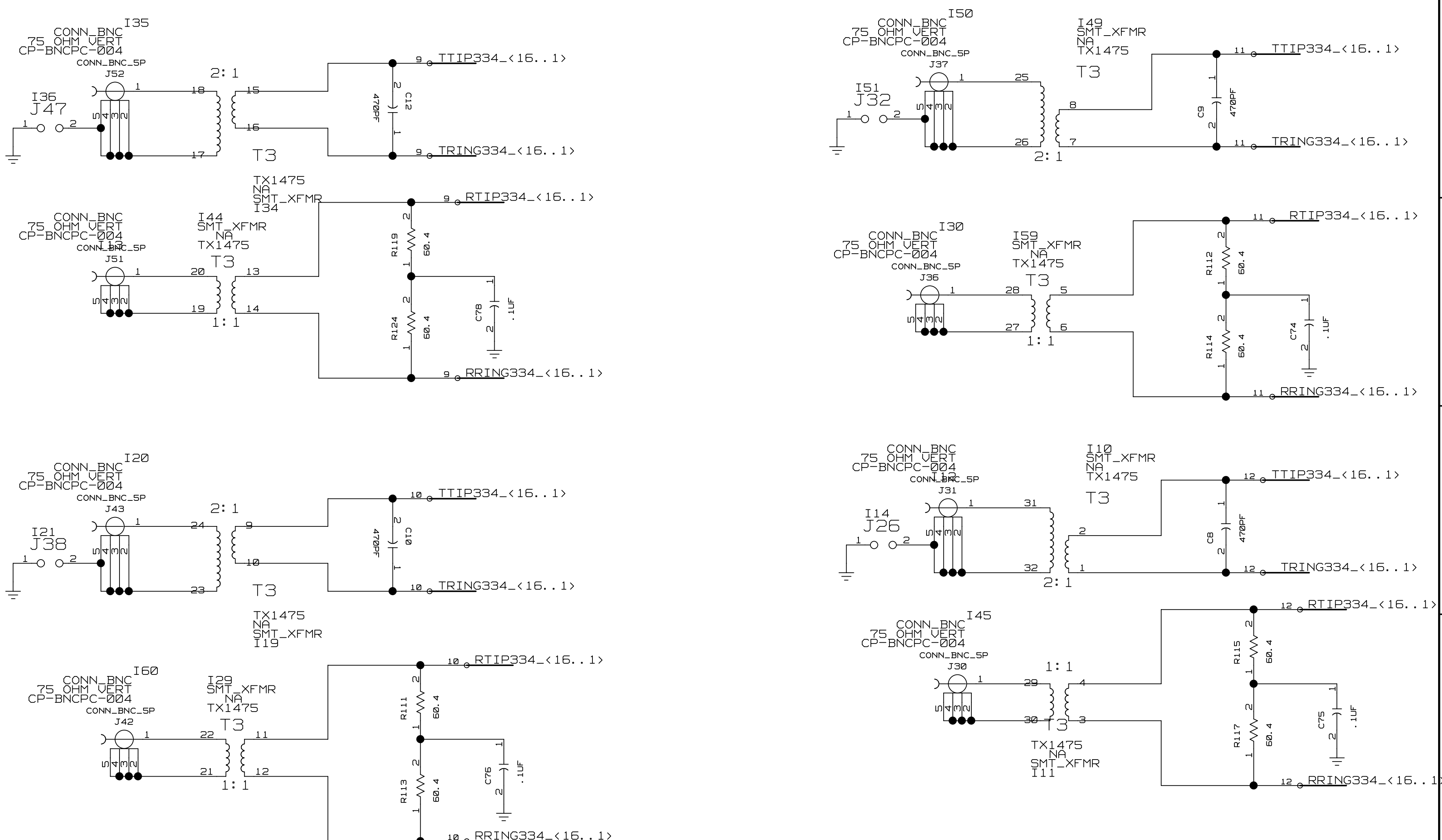


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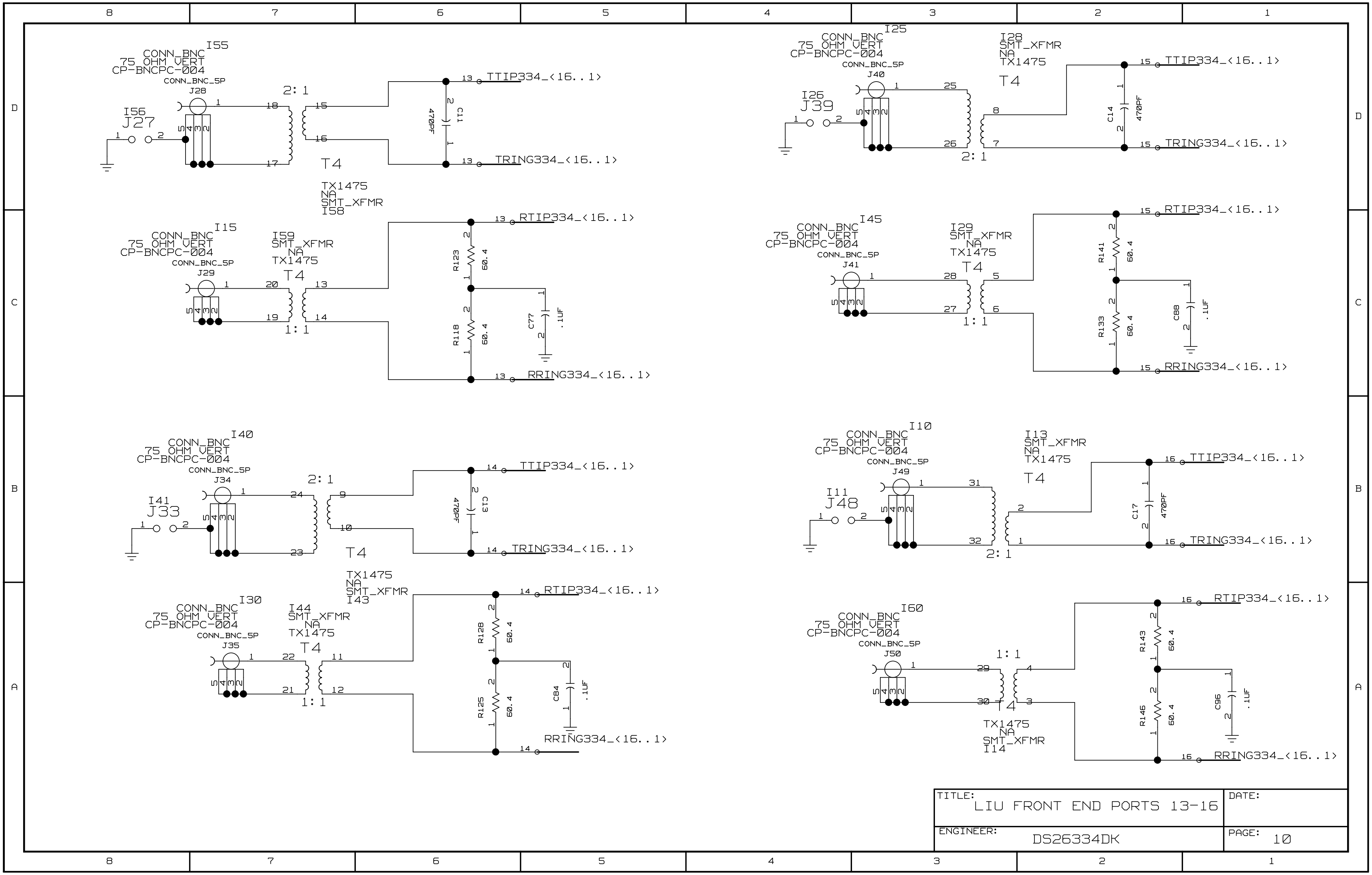


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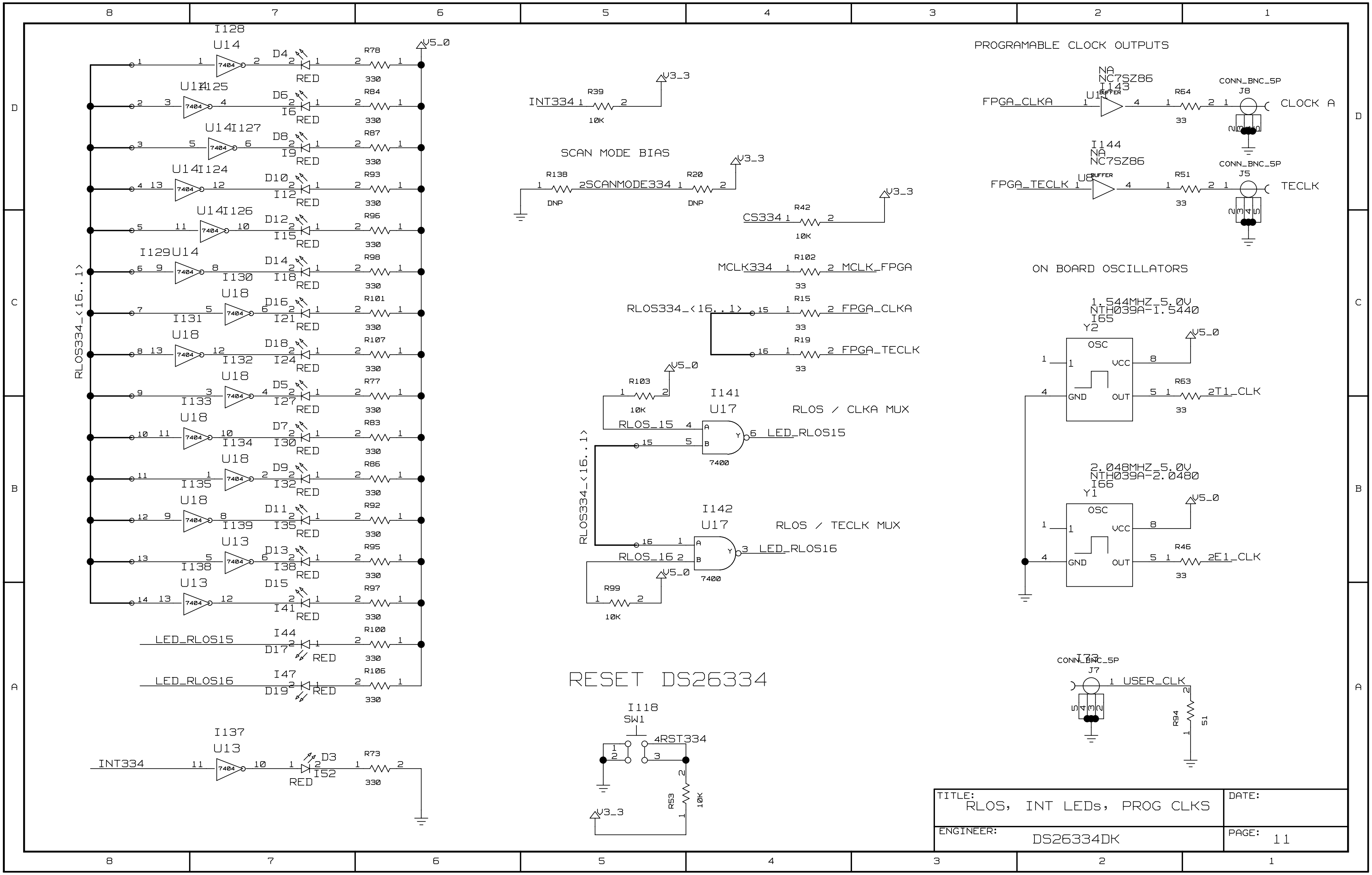


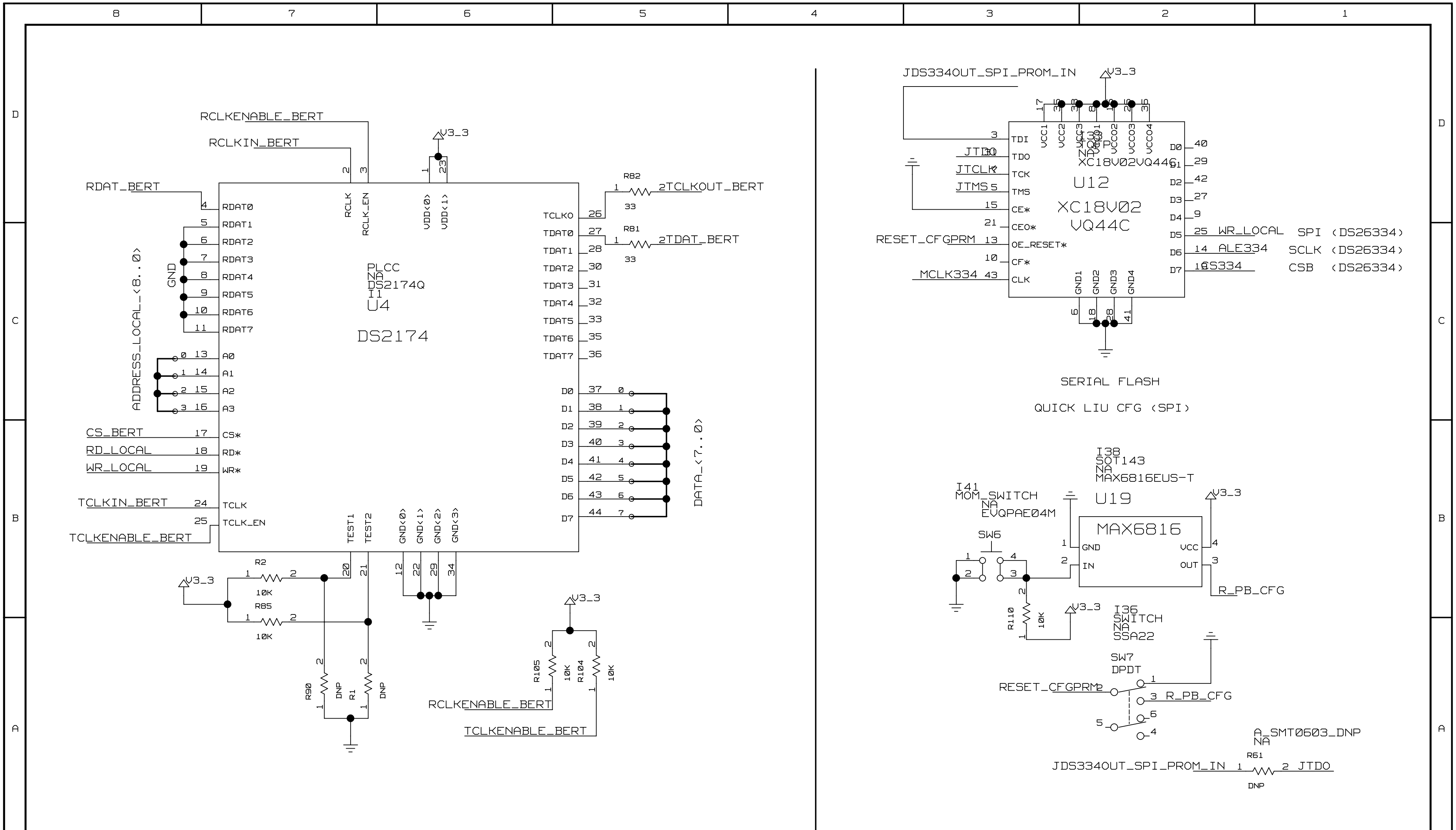
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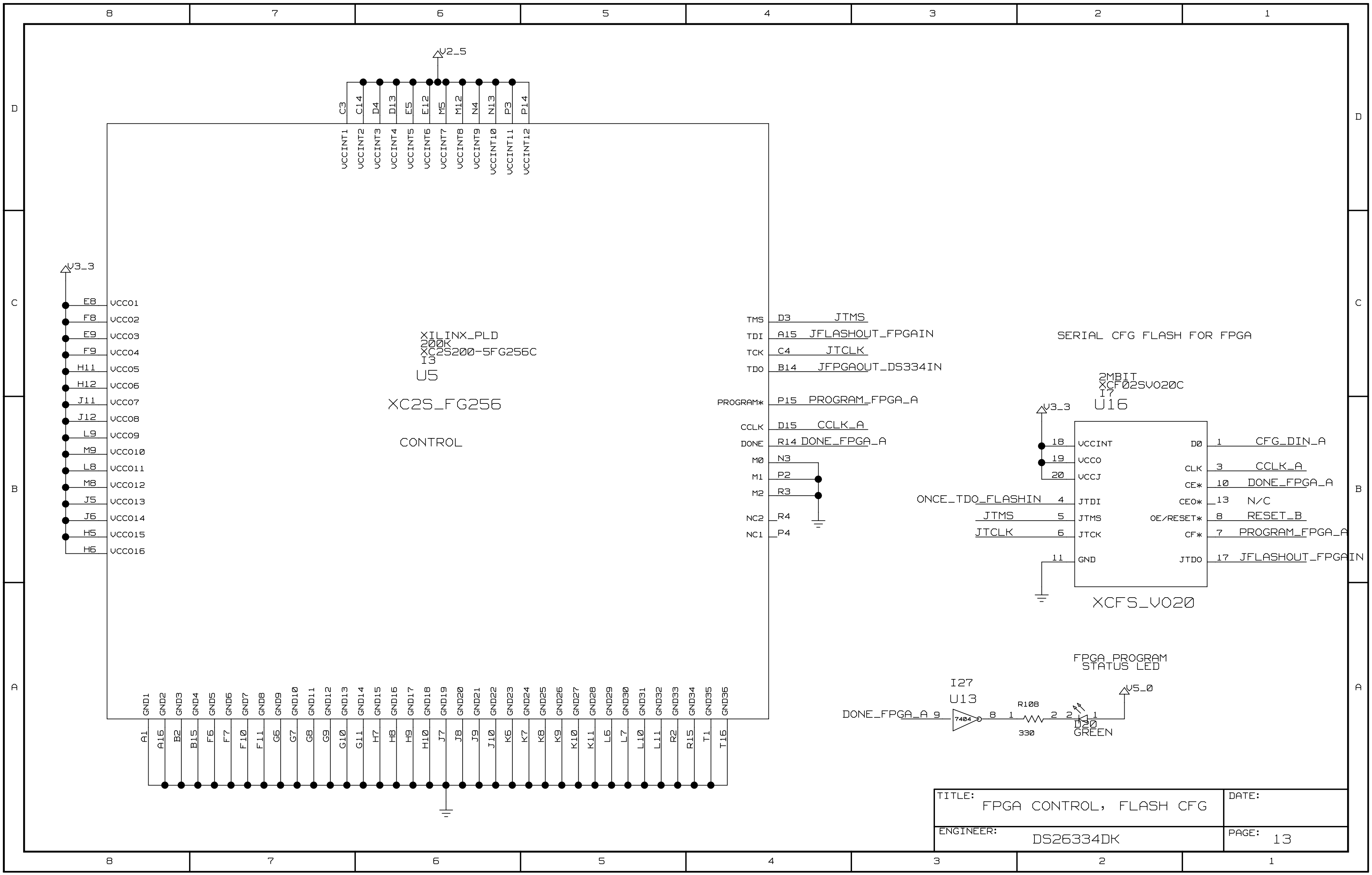
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PROGRAMABLE CLOCK OUTPUTS
FPGA_CLKA
CLOCK A
FPGA_TECLK
TECLK
NC7SZ86
CONN_BNC_5P
SCAN MODE BIAS
INT334
SCANMODE334
CS334
MCLK334
MCLK_FPGA
RLOS334_<16..1>
FPGA_CLKA
FPGA_TECLK
RLOS / CLKA MUX
RLOS / TECLK MUX
RLOS_15
RLOS_16
LED_RLOS15
LED_RLOS16
ON BOARD OSCILLATORS
1.544MHZ_5.0V
NTH039A-1.5440
2.048MHZ_5.0V
NTH039A-2.0480
OSC
T1_CLK
E1_CLK
USER_CLK
RESET DS26334
RST334
TITLE: RLOS, INT LEDs, PROG CLKS
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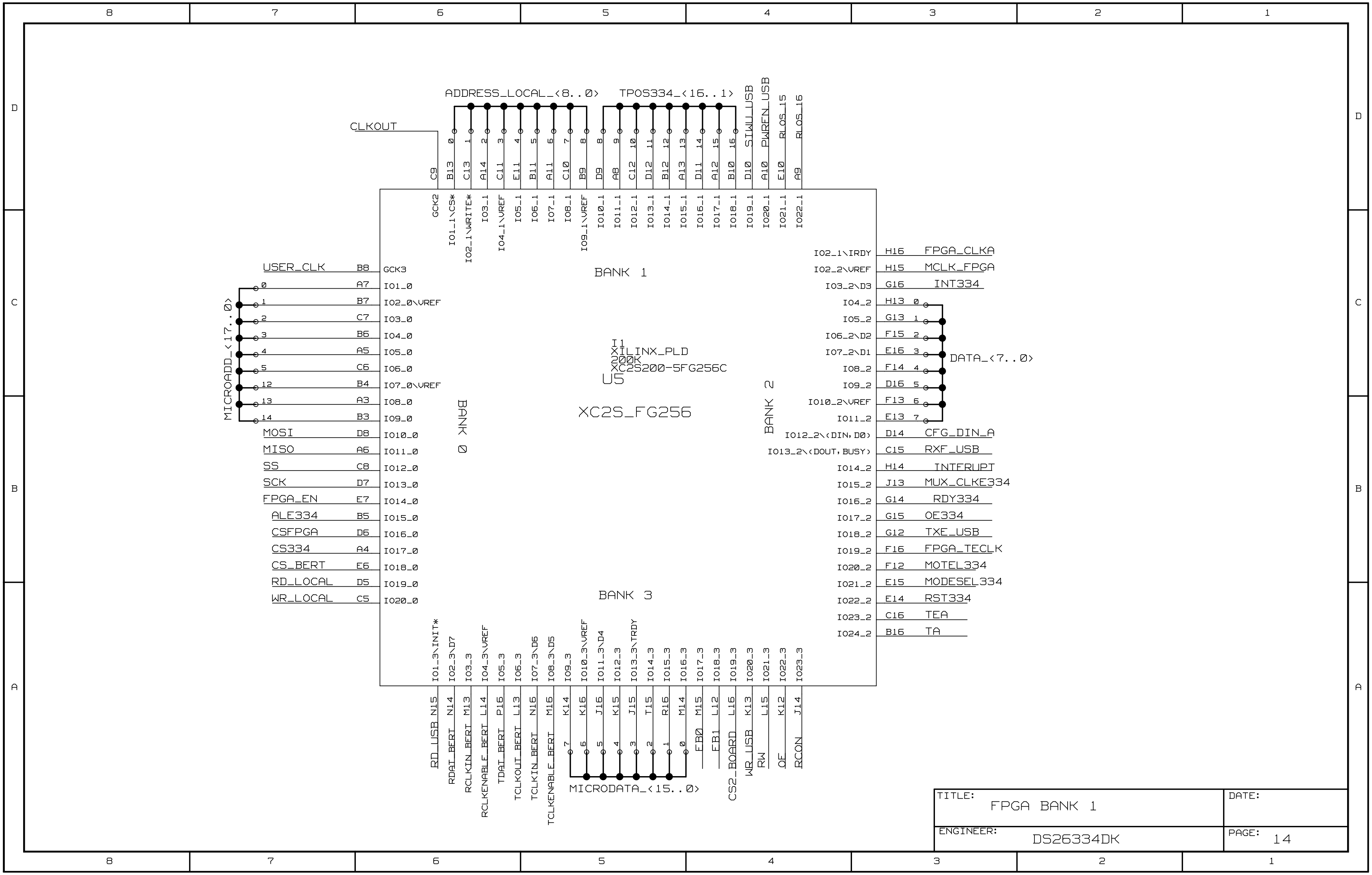


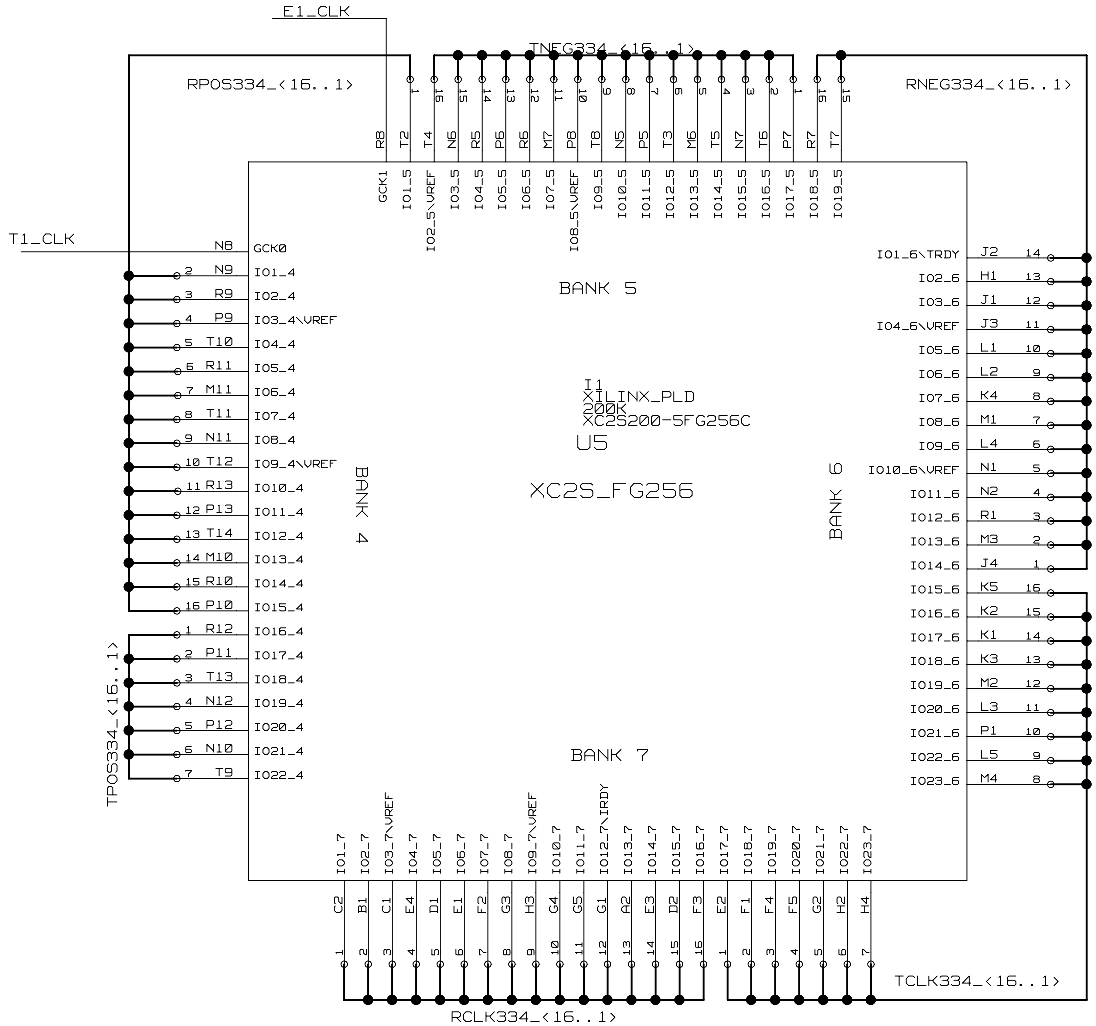
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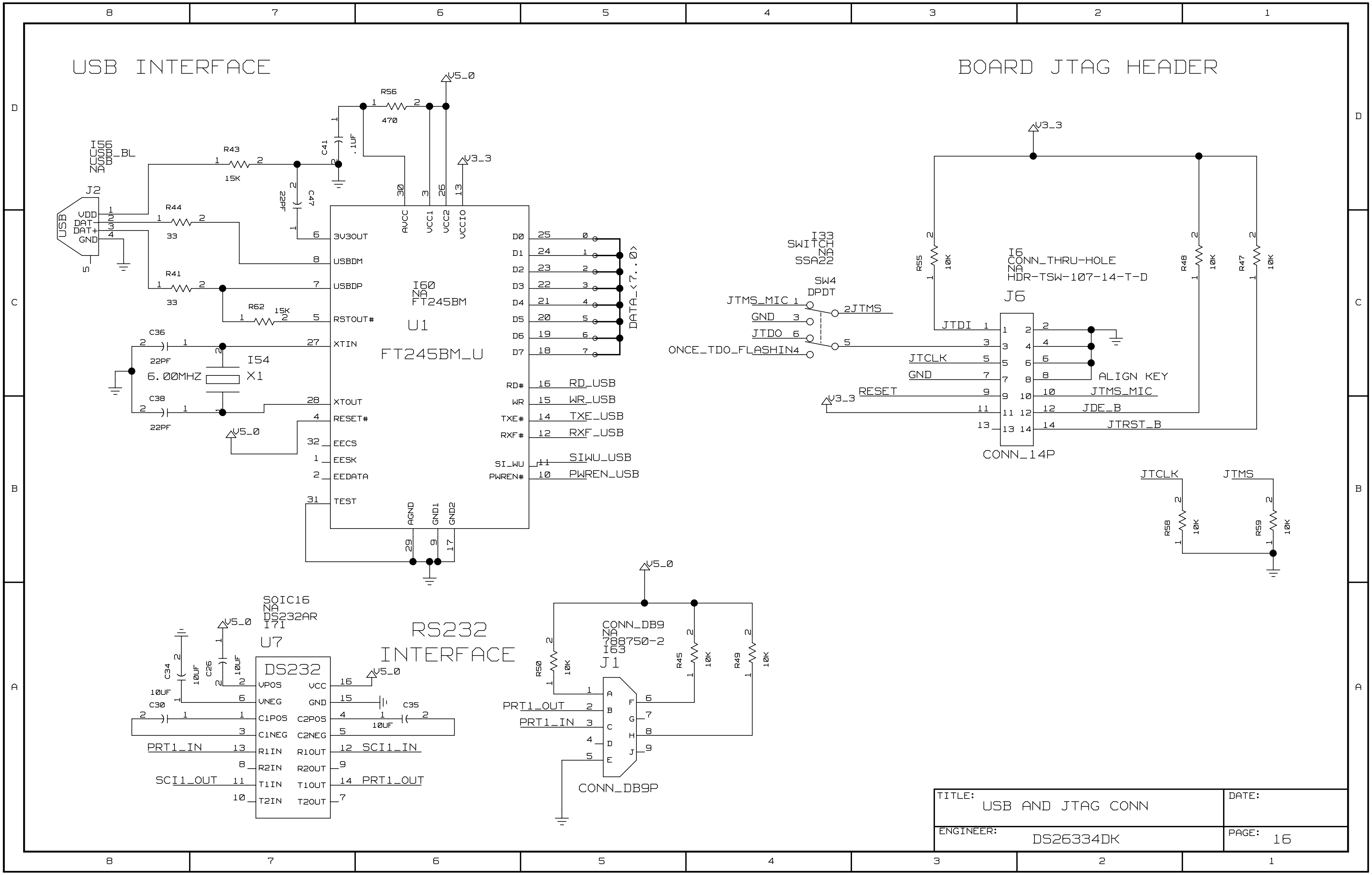
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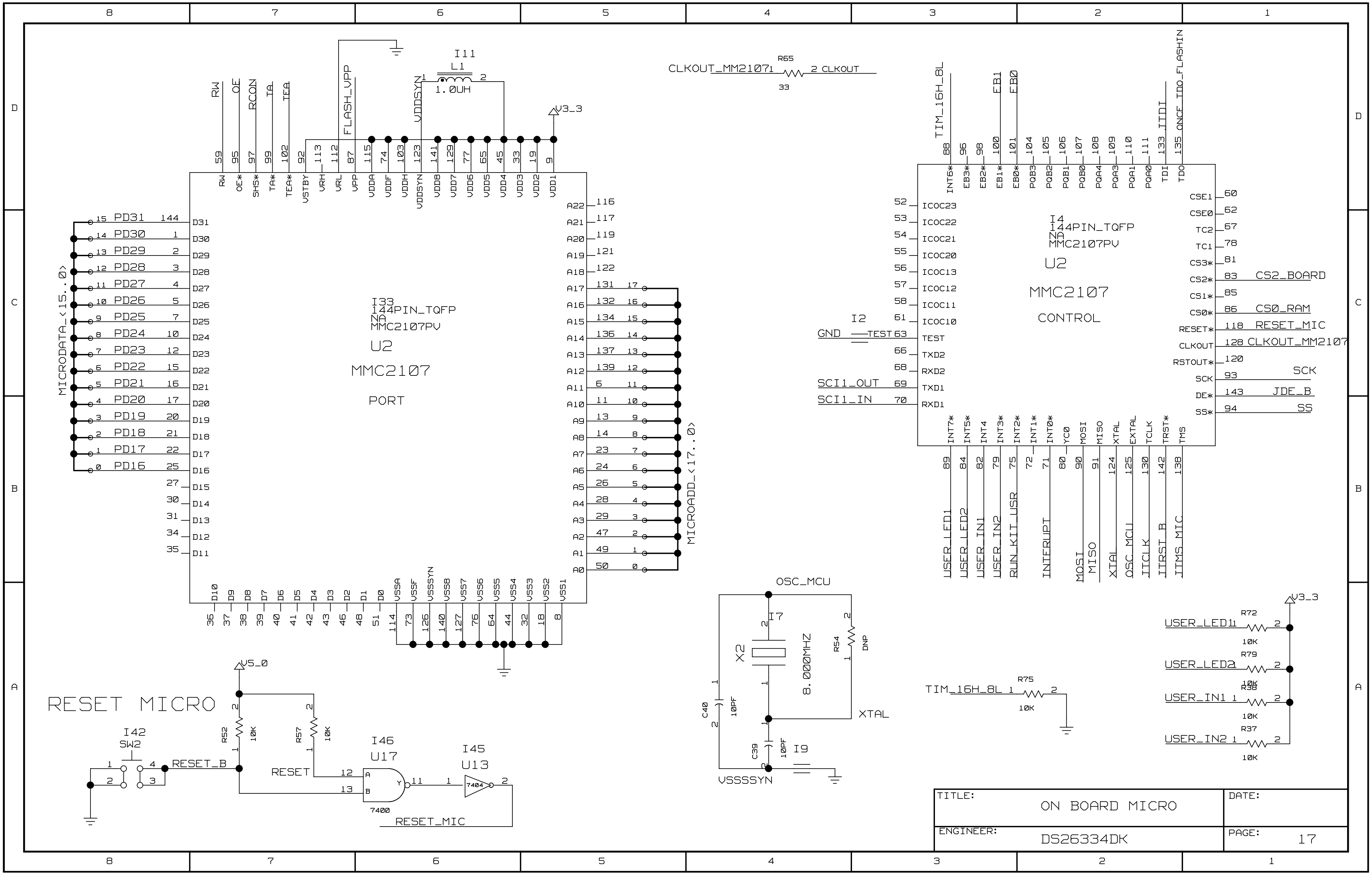

ADDRESS_LOCAL_<8..0>
TPOS334_<16..1>
SIWU_USB
PWREN_USB
RLOS_15
RLOS_16
CLKOUT
BANK 1
BANK 0
BANK 2
BANK 3
I1
XILINX_PLD
200K
XC2S200-5FG256C
U5
XC2S_FG256
USER_CLK
MICROADD_<17..0>
MOSI
MISO
SS
SCK
FPGA_EN
ALE334
CSFPGA
CS334
CS_BERT
RD_LOCAL
WR_LOCAL
FPGA_CLKA
MCLK_FPGA
INT334
DATA_<7..0>
CFG_DIN_A
RXF_USB
INTERUPT
MUX_CLKE334
RDY334
OE334
TXE_USB
FPGA_TECLK
MOTEL334
MODESEL334
RST334
TEA
TA
RD_USB
RDAT_BERT
RCLKIN_BERT
RCLKENABLE_BERT
TDAT_BERT
TCLKOUT_BERT
TCLKIN_BERT
TCLKENABLE_BERT
MICRODATA_<15..0>
FB0
FB1
CS2_BOARD
WR_USB
RW
OE
RCON
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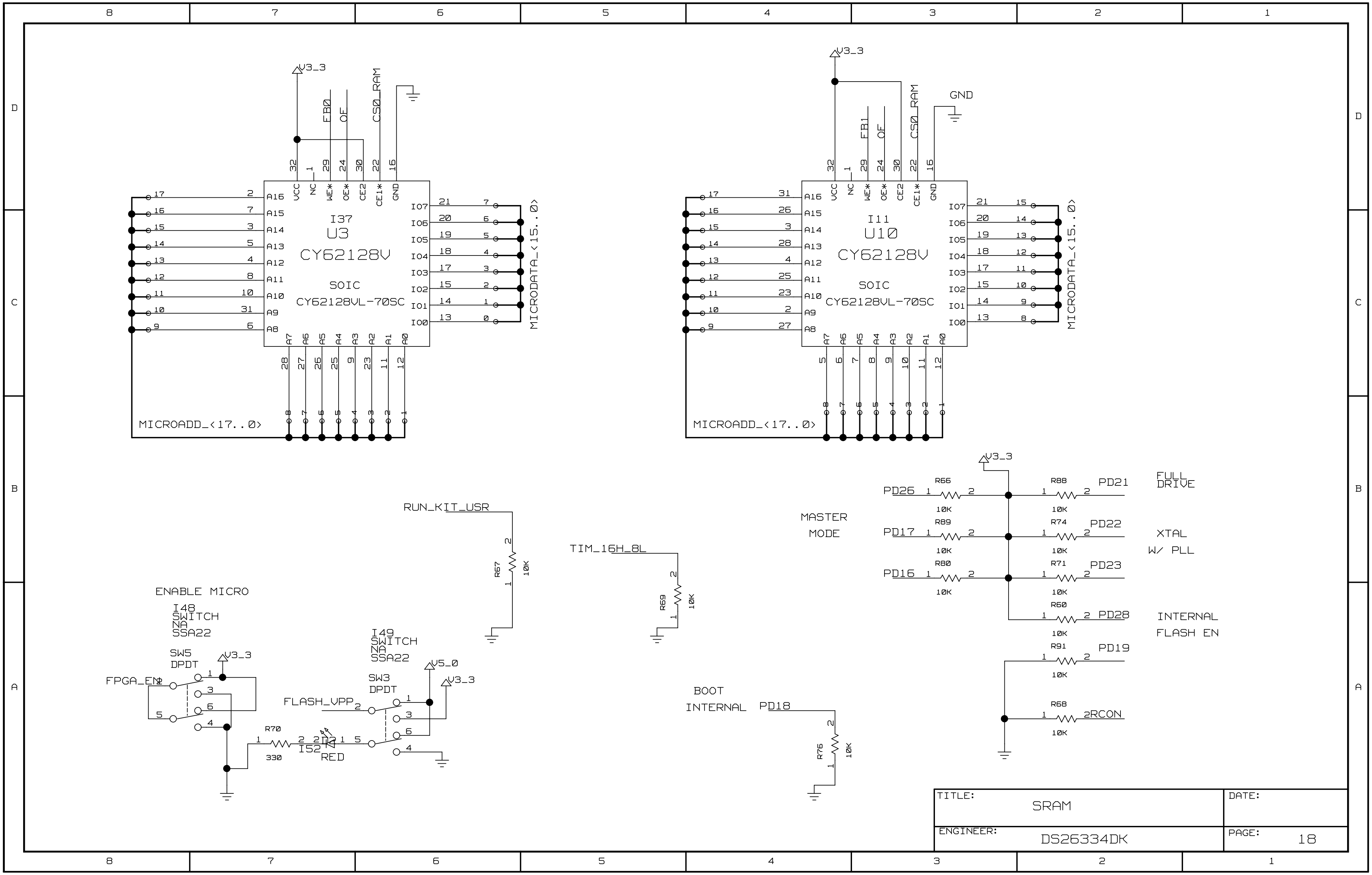
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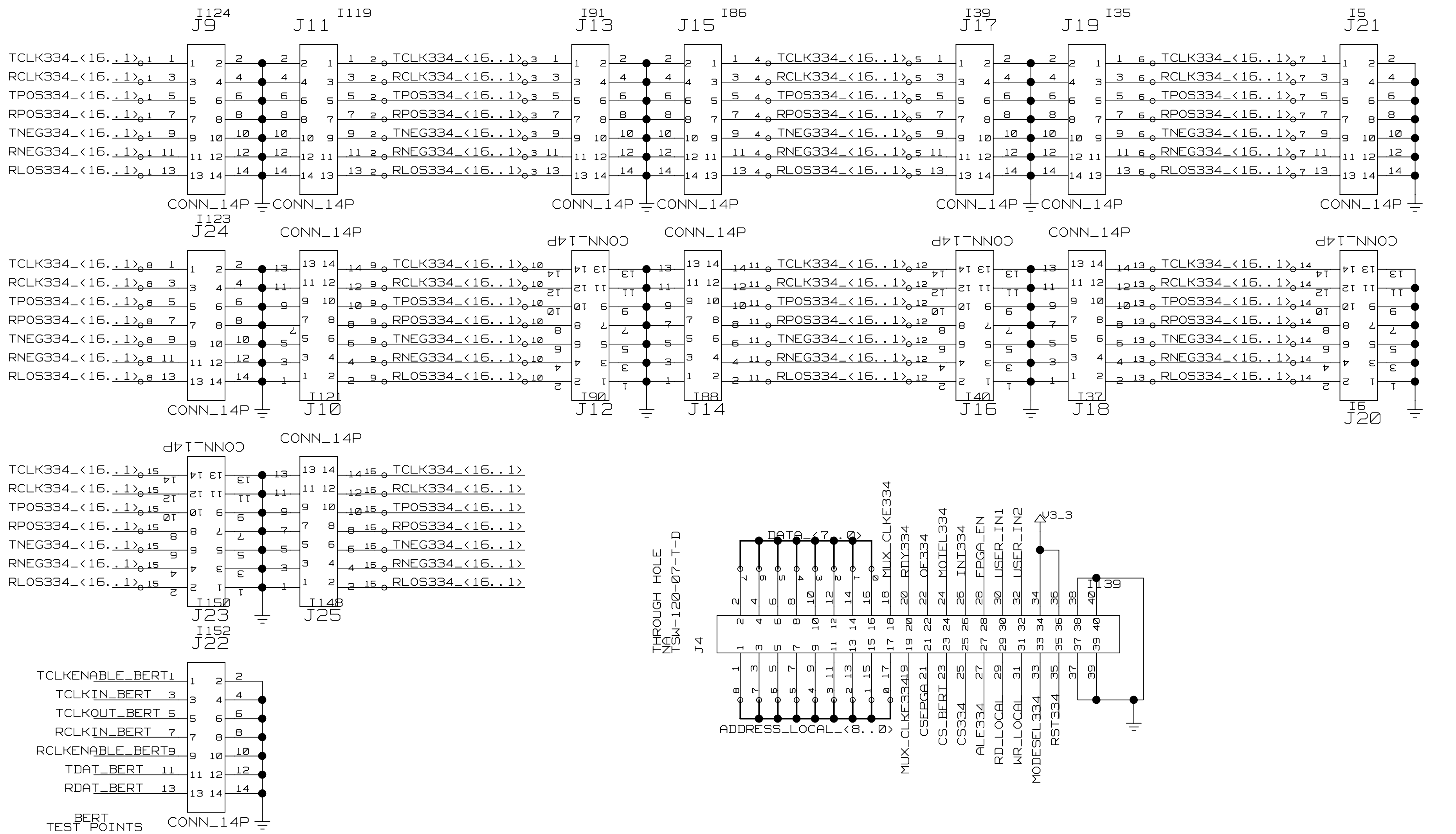
USB INTERFACE
BOARD JTAG HEADER
RS232 INTERFACE
I56 USB_BL USB NA
J2 USB VDD DAT- DAT+ GND
R43 15K
R44 33
R41 33
R62 15K
R56 470
C41 .1UF
C47 22PF
C36 22PF
C38 22PF
I54 6.00MHZ X1
V5_0
V3_3
I60 NA FT245BM
U1
FT245BM_U
3V3OUT USBDM USBDP RSTOUT# XTIN XTOUT RESET# EECS EESK EEDATA TEST
AVCC VCC1 VCC2 VCCIO AGND GND1 GND2
D0 D1 D2 D3 D4 D5 D6 D7
DATA_<7..0>
RD# WR TXE# RXF# SI_WU PWREN#
RD_USB
WR_USB
TXE_USB
RXF_USB
SIWU_USB
PWREN_USB
I33 SWITCH NA SSA22
SW4 DPDT
JTMS_MIC
GND
JTDO
ONCE_TDO_FLASHIN
JTMS
I6 CONN_THRU-HOLE NA HDR-TSW-107-14-T-D
J6
JTDI
JTCLK
RESET
ALIGN KEY
JTMS_MIC
JDE_B
JTRST_B
CONN_14P
R55 10K
R48 10K
R47 10K
R58 10K
R59 10K
SOIC16 NA DS232AR I71
U7
DS232
VPOS VNEG C1POS C1NEG R1IN R2IN T1IN T2IN
VCC GND C2POS C2NEG R1OUT R2OUT T1OUT T2OUT
C34 10UF
C26 10UF
C30
C35 10UF
PRT1_IN
SCI1_OUT
SCI1_IN
PRT1_OUT
CONN_DB9 NA 788750-2 I63
J1
CONN_DB9P
R50 10K
R45 10K
R49 10K
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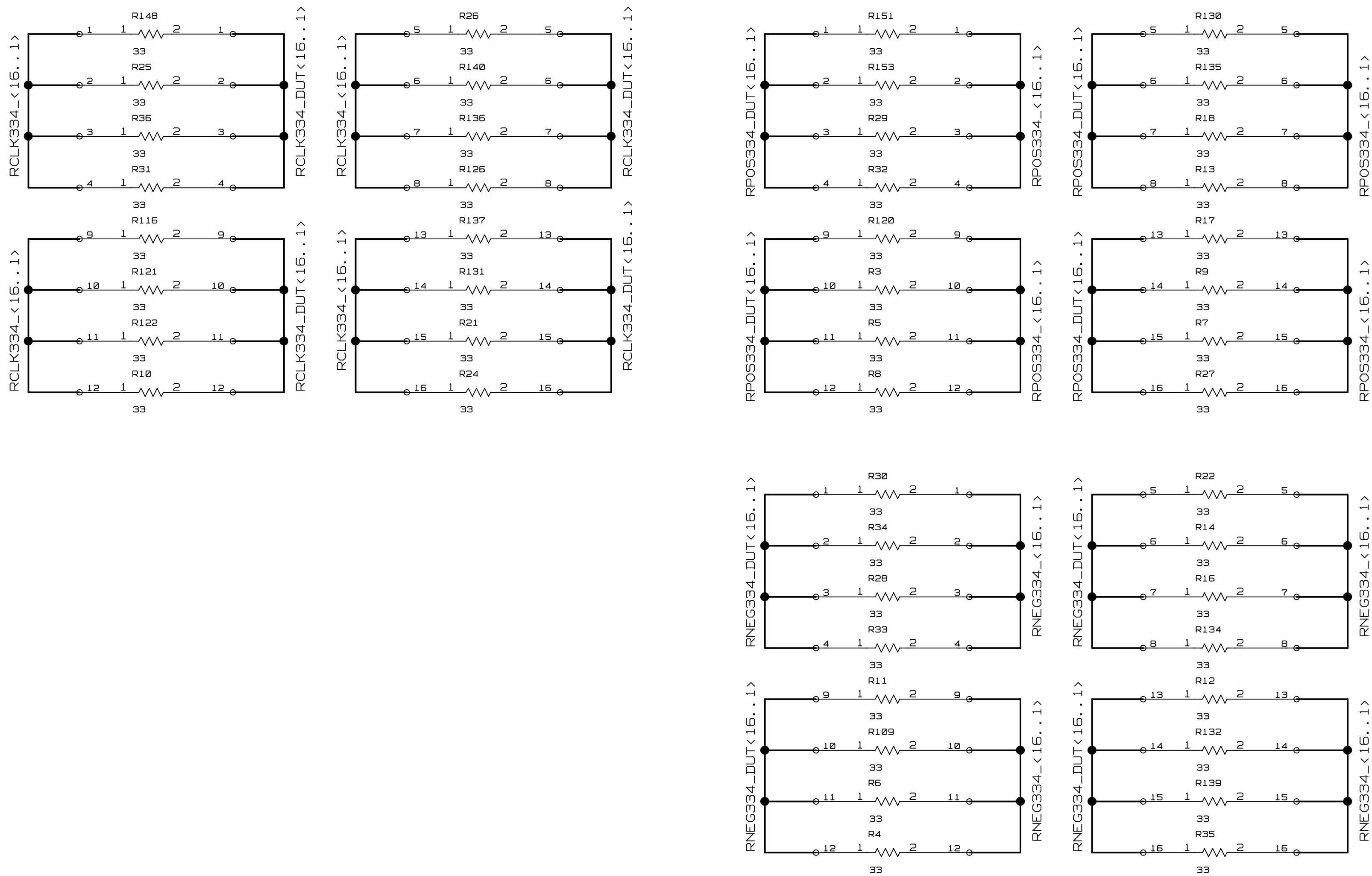
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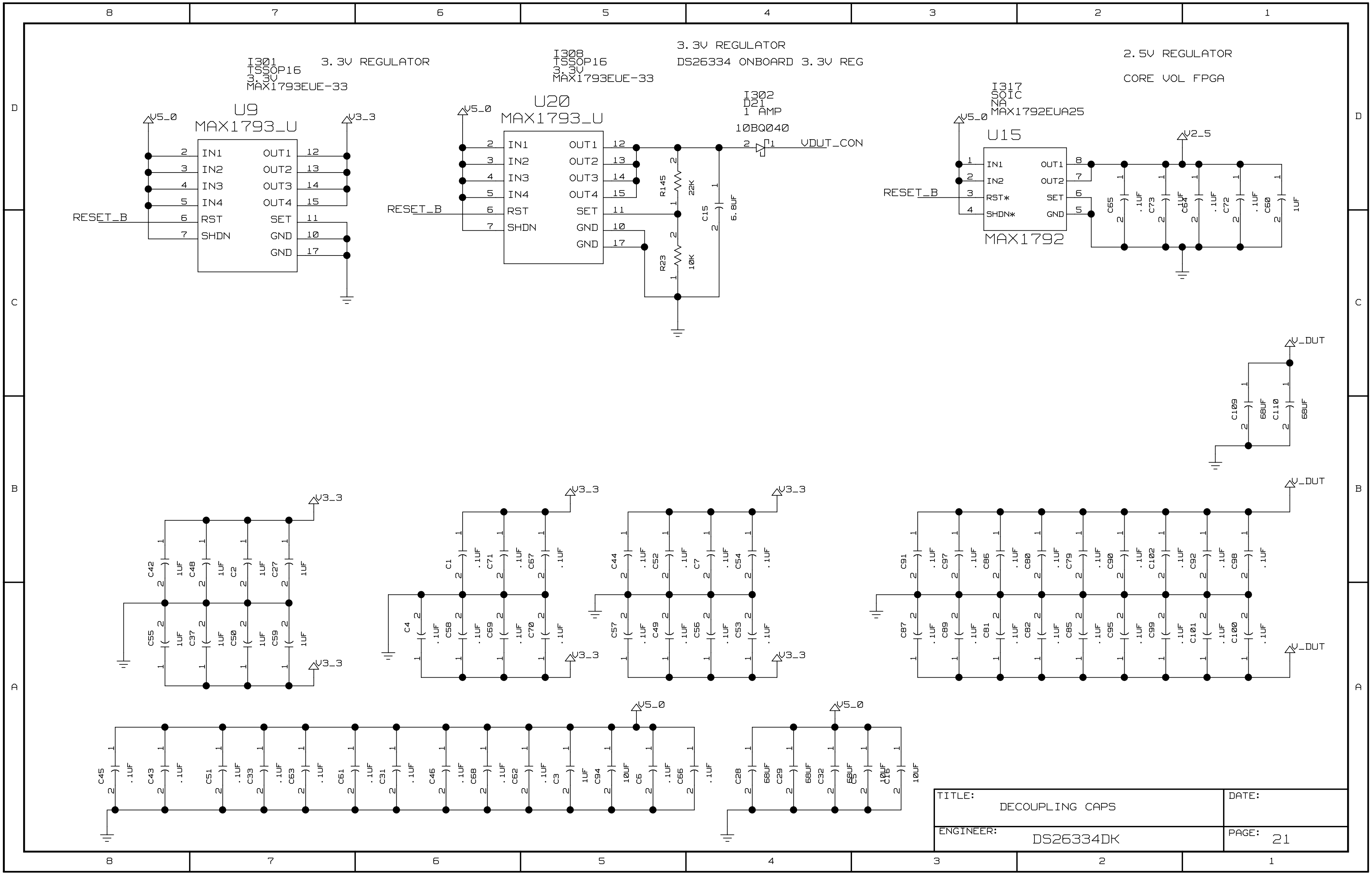
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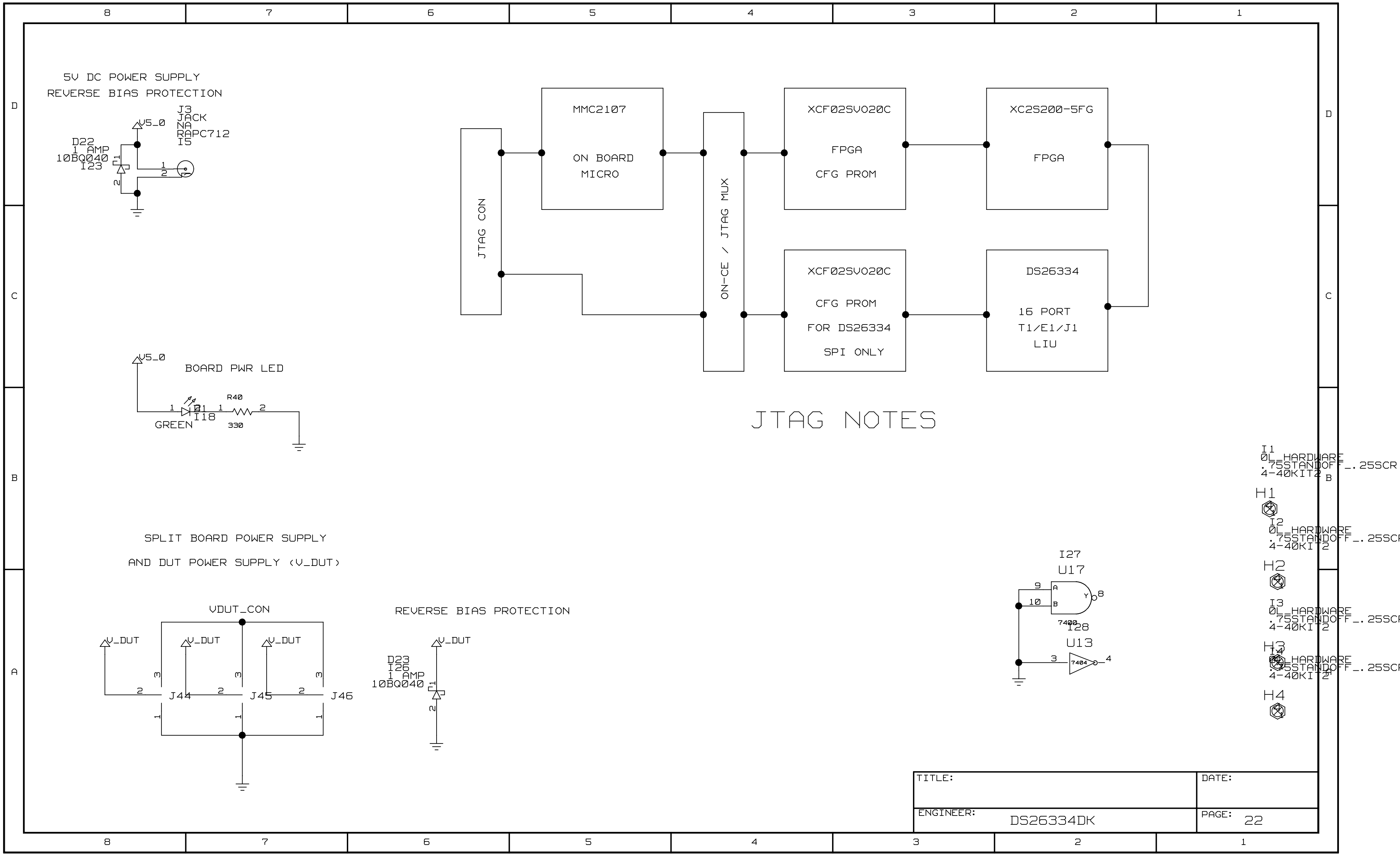
TITLE: TEST POINTS	DATE:
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TITLE: LIU SERIES TERMINATION	DATE:
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5V DC POWER SUPPLY
REVERSE BIAS PROTECTION
V5_0
J3
JACK
NA
RAPC712
I5
D22
1 AMP
10BQ040
I23
MMC2107
ON BOARD
MICRO
JTAG CON
ON-CE / JTAG MUX
XCF02SV020C
FPGA
CFG PROM
XC2S200-5FG
FPGA
XCF02SV020C
CFG PROM
FOR DS26334
SPI ONLY
DS26334
16 PORT
T1/E1/J1
LIU
BOARD PWR LED
R40
330
GREEN
I18
JTAG NOTES
I1
0L_HARDWARE
.75STANDOFF_.25SCR
4-40KIT2
H1
H2
H3
H4
SPLIT BOARD POWER SUPPLY
AND DUT POWER SUPPLY (V_DUT)
VDUT_CON
V_DUT
J44
J45
J46
REVERSE BIAS PROTECTION
D23
I26
1 AMP
10BQ040
I27
U17
7400
I28
U13
7404
TITLE:
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DS26334DK
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```
*** Signal Cross-Reference for the entire design ***

ADDRESS_LOCAL_<8..0>  2B3 12C8 14D6 19A5
ALE334              12C1> 14B7<> 19A3<> 2C7<
CCLK_A              13B3<> 13B1<
CFG_DIN_A           13B1> 14B3<>
CLKOUT              14D7< 17D3<
CLKOUT_MM2107       17C1<> 17D4<
CS0_RAM             17C1<> 18D3< 18D6<
CS2_BOARD           14A4<> 17C1<>
CS334               12C1> 14B7<> 19A3<> 2C7< 11C4<
CSFPGA              14B7<> 19A3<>
CS_BERT             14B7<> 19A3<> 12B8<
DATA_<7..0>         2B3 12B5 14C3 16C5 19B4
DONE_FPGA_A         13B3<> 13A3< 13B1<
E1_CLK              11B1< 15D6<
EB0                 14A4<> 17D3<> 18D7<
EB1                 14A4<> 17D3<> 18D3<
FLASH_VPP           18A7<> 17D7<
FPGA_CLKA           11D3<> 14C3<> 11C3<
FPGA_EN             14B7<> 18A8<> 19B3<>
FPGA_TECLK          11D3<> 14B3<> 11C3<
INT334              2B7> 14C3<> 19B3<> 11A8< 11D5<
INTERUPT            14B3<> 17B2<>
JDE_B               16B2<> 17B1<>
JDS334OUT_SPI_PROM_IN  2B7> 12A2< 12D3<
JFLASHOUT_FPGAIN    13B1> 13C3<
JFPGAOUT_DS334IN    13C3> 2B7<
JTCLK               12D3> 16C3<> 17B2<> 2B7< 13B3<
                  13C3< 16B2<
JTDI                16C3<> 17D2<>
JTDO                12D3> 16C4<> 12A1<
JTMS                16C3<> 2B7< 12D3< 13B3< 13C3<
                  16B1<
JTMS_MIC            16B2<> 16C4<> 17B2<>
JTRST_B             16B2<> 17B2<> 2B7<
LED_RLOS15          11A8<> 11B4>
LED_RLOS16          11A8<> 11B4>
MCLK334             2C3< 11C4< 12C3<
MCLK_FPGA           14C3<> 11C3<
MICROADD_<17..0>  14B7 17B4 18B4 18B8
MICRODATA_<15..0>  14A5 17B8 18C2 18C5
MISO                14B7<> 17A2<>
MODESEL334          14B3<> 19A3<> 2C7<
MOSI                14B7<> 17A2<>
MOTEL334            14B3<> 19B3<> 2C7<
MUX_CLKE334         14B3<> 19A4<> 19B4<> 2B7<
OE                  14A4<> 17D7<> 18D3< 18D7<
OE334               14B3<> 19B3<> 2B7<
ONCE_TDO_FLASHIN  16C4<> 17D2<> 13B3<
OSC_MCU             17B2<> 17B4<>
PD16                17B8<> 18B3<
PD17                17B8<> 18B3<
PD18                17B8<> 18A4<
PD19                17B8<> 18A2<
PD20                17B8<>
PD21                17C8<> 18B2<
PD22                17C8<> 18B2<
PD23                17C8<> 18B2<
PD24                17C8<>
PD25                17C8<>
PD26                17C8<> 18B3<
PD27                17C8<>
PD28                17C8<> 18A2<
PD29                17C8<>
PD30                17C8<>
PD31                17C8<>
PROGRAM_FPGA_A      13B1> 13B3<
PRT1_IN             16A6<> 16A8<
PRT1_OUT            16A6<> 16A6>
PWREN_USB           14D4<> 16B5>
RCLK334_<16..1>  19B6> 15A6 19B8< 19C2 19C4 19C6
                  19C8< 19D2 19D4 19D6 19D8< 20C6 20C6
                  20C8 20C8
RCLK334_DUT<16..1>  3B5< 3B8< 3C5< 3C8< 4B4< 4B8<
                  4C4< 4C8< 5B4< 5B8< 5C4< 5C8< 6B4<
                  6B8< 6C5< 6C8< 20C5 20C5 20C7 20C7
```

```
RCLKENABLE_BERT  14A6<> 19A8<> 12A6< 12D7<
RCLKIN_BERT      14A6<> 19A8<> 12D7<
RCON             14A4<> 17D7<> 18A2<
RDAT_BERT        14A6<> 19A8<> 12D8<
RDY334           2B7> 14B3<> 19B4<>
RD_LOCAL         14B7<> 19A3<> 2C7< 12B8<
RD_USB           14A6<> 16C5>
RESET            16B3<> 17A7<
RESET_B          13B1<> 17A8<> 21C6> 21C8> 21D3>
RESET_CFGPRM     12A3<> 12C3<>
RESET_MIC        17A6> 17C1<>
RLOS334_<16..1>  19B6> 3A4< 3A8< 3C4< 3C8< 4A4<
               4A8< 4C4< 4C8< 5A4< 5A8< 5C4< 5C8<
               6A4< 6A8< 6C4< 6C8< 11B5 11C5 11C8
               19B8< 19C2 19C4 19C6 19C8< 19D2 19D4
               19D6 19D8<
RLOS_15          14D4<> 11B5<
RLOS_16          14D4<> 11B5<
RNEG334_<16..1>  19B6> 15D4 19B8< 19C2 19C4 19C6
               19C8< 19D2 19D4 19D6 19D8< 20A1 20A3
               20B1 20B3
RNEG334_DUT<16..1>  3B5< 3B8< 3C5< 3C8< 4B4< 4B8<
               4C4< 4C8< 5B4< 5B8< 5C4< 5C8< 6B4<
               6B8< 6C5< 6C8< 20A3 20A4 20B3 20B4
RPOS334_<16..1>  19B6> 15D7 19B8< 19C2 19C4 19C6
               19C8< 19D2 19D4 19D6 19D8< 20C1 20C1
               20C3 20C3
RPOS334_DUT<16..1>  3B5< 3B8< 3C5< 3C8< 4B4< 4B8<
               4C4< 4C8< 5B4< 5B8< 5C4< 5C8< 6B4<
               6B8< 6C5< 6C8< 20C3 20C3 20C4 20C4
RRING334_<16..1>  7A1> 7A4> 7C1> 7C5> 8A1> 8A5>
               8B5> 8C1> 9A1> 9A5> 9C1> 9C5> 10A1>
               10A5> 10C1> 10C5> 3B4< 3B8< 3D5<
               3D8< 4B4< 4B8< 4D4< 4D8< 5B4< 5B8<
               5D4< 5D8< 6B4< 6B8< 6D4< 6D8<
RST334           11A5<> 14A3<> 19A3<> 2B7<
RTIP334_<16..1>  7B1> 7B4> 7C1> 7C5> 8A1> 8A5> 8C1>
               8C5> 9A5> 9B1> 9C1> 9C5> 10A1> 10A5>
               10C1> 10C5> 3B4< 3B8< 3C4< 3C8< 4B4<
               4B8< 4C4< 4C8< 5B4< 5B8< 5C4< 5C8<
               6B4< 6B8< 6C4< 6C8<
RUN_KIT_USR      17B3<> 18B6<
RW               14A4<> 17D7<>
RXF_USB          14B3<> 16B5>
R_PB_CFG         12A2<> 12B2>
SCANMODE334      2C3< 11D5<
SCI1_IN          16A6> 17B4<>
SCI1_OUT         17C4<> 16A8<
SCK              14B7<> 17C1<>
SIWU_USB         14D4<> 16B5>
SS               14B7<> 17B1<>
T1_CLK           11B1< 15C7<
TA               14A3<> 17D7<>
TCLK334_<16..1>  3B1> 3B5> 3C1> 3C5> 4B1> 4B5> 4C1>
               4C5> 5B1> 5B5> 5C1> 5C5> 6B1> 6B5>
               6C1> 6C5> 19B6> 15A4 19B8< 19C2 19C4
               19C6 19C8< 19D2 19D4 19D6 19D8<
TCLKENABLE_BERT  14A5<> 19A8<> 12A6< 12B8<
TCLKIN_BERT      14A5<> 19A8<> 12B8<
TCLKOUT_BERT     14A6<> 19A8<> 12D5<
TDAT_BERT        14A6<> 19A8<> 12C5<
TEA              14A3<> 17D7<>
TEST             17C3<>
TIM_16H_8L       17D3<> 17A3< 18B5<
TNEG334_<16..1>  3B1> 3B5> 3C1> 3C5> 4B1> 4B5> 4C1>
               4C5> 5B1> 5B5> 5C1> 5C5> 6B1> 6B5>
               6C1> 6C5> 19B6> 15D5 19B8< 19C2 19C4
               19C6 19C8< 19D2 19D4 19D6 19D8<
TPOS334_<16..1>  3B1> 3B5> 3C1> 3C5> 4B1> 4B5> 4C1>
               4C5> 5B1> 5B5> 5C1> 5C5> 6B1> 6B5>
               6C1> 6C5> 19B6> 14D5 15A7 19B8< 19C2
               19C4 19C6 19C8< 19D2 19D4 19D6 19D8<
```

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TRING334_<16..1>  3B1> 3B5> 3D1> 3D5> 4B1> 4B5>
               4D1> 4D5> 5B1> 5B5> 5D1> 5D5> 6B1>
               6B5> 6D1> 6D5> 7B1> 7B5> 7D1> 7D5>
               8B1> 8B5> 8D1> 8D5> 9B1> 9B5> 9D1>
               9D5> 10B1> 10B5> 10D1> 10D5>
TTIP334_<16..1>  3B1> 3B5> 3C1> 3C5> 4B1> 4B5> 4C1>
               4C5> 5B1> 5B5> 5C1> 5C5> 6B1> 6B5>
               6C1> 6C5> 7B1> 7B5> 7D1> 7D5> 8B1>
               8B5> 8D1> 8D5> 9B1> 9B5> 9D1> 9D5>
               10B1> 10B5> 10D1> 10D5>
TXE_USB          14B3<> 16B5<
USER_CLK         11A2<> 14C7<
USER_IN1         17B3<> 19B3<> 17A2<
USER_IN2         17B3<> 19B3<> 17A2<
USER_LED1        17B3<> 17A2<
USER_LED2        17B3<> 17A2<
VDDSYN           17D6<>
VDUT_CON         21D4<> 22A7<>
VSSSSYN          17A4<
WR_LOCAL         12C1> 14A7<> 19A3<> 2B7< 12B8<
WR_USB           14A4<> 16B5>
XTAL             17A3<> 17B2<>
```

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*** Part Cross-Reference for the entire design ***

C1	CAP1	21B6
C2	CAP1	21B7
C3	CAP1	21A5
C4	CAP1	21A6
C5	CAP1	21A3
C6	CAP1	21A5
C7	CAP1	21B4
C8	CAP1	9B2
C9	CAP1	9D2
C10	CAP1	9B6
C11	CAP1	10D6
C12	CAP1	9D6
C13	CAP1	10B6
C14	CAP1	10D2
C15	CAP1	21C4
C16	CAP1	21A3
C17	CAP1	10B2
C18	CAP1	7D6
C19	CAP1	7D2
C20	CAP1	7B2
C21	CAP1	7B6
C22	CAP1	8D6
C23	CAP1	8B6
C24	CAP1	8B2
C25	CAP1	8D2
C26	CAP1	16A7
C27	CAP1	21B7
C28	CAP1	21A4
C29	CAP1	21A4
C30	CAP1	16A8
C31	CAP1	21A6
C32	CAP1	21A4
C33	CAP1	21A7
C34	CAP1	16A8
C35	CAP1	16A6
C36	CAP1	16C8
C37	CAP1	21A7
C38	CAP1	16B8
C39	CAP1	17A4
C40	CAP1	17A4
C41	CAP1	16D7
C42	CAP1	21B8
C43	CAP1	21A8
C44	CAP1	21B5
C45	CAP1	21A8
C46	CAP1	21A6
C47	CAP1	16D7
C48	CAP1	21B7
C49	CAP1	21A5
C50	CAP1	21A7
C51	CAP1	21A7
C52	CAP1	21B5
C53	CAP1	21A4
C54	CAP1	21B4
C55	CAP1	21A8
C56	CAP1	21A4
C57	CAP1	21A5
C58	CAP1	21A6
C59	CAP1	21A7
C60	CAP1	21C1
C61	CAP1	21A7
C62	CAP1	21A6
C63	CAP1	21A7
C64	CAP1	21C1
C65	CAP1	21C2
C66	CAP1	21A5
C67	CAP1	21B5
C68	CAP1	21A6
C69	CAP1	21A6
C70	CAP1	21A5
C71	CAP1	21B6
C72	CAP1	21C1
C73	CAP1	21C2
C74	CAP1	9C1
C75	CAP1	9A1
C76	CAP1	9A6
C77	CAP1	10C5
C78	CAP1	9C6
C79	CAP1	21B2
C80	CAP1	21B2
C81	CAP1	21A3
C82	CAP1	21A2
C83	CAP1	8C2
C84	CAP1	10A5
C85	CAP1	21A2
C86	CAP1	21B3
C87	CAP1	21A3
C88	CAP1	10C2
C89	CAP1	21A3
C90	CAP1	21B2
C91	CAP1	21B3
C92	CAP1	21B1
C93	CAP1	8A1
C94	CAP1	21A5
C95	CAP1	21A2
C96	CAP1	10A1
C97	CAP1	21B3
C98	CAP1	21B1
C99	CAP1	21A2
C100	CAP1	21A1
C101	CAP1	21A1
C102	CAP1	21B2
C103	CAP1	8A5
C104	CAP1	7C5
C105	CAP1	8C5
C106	CAP1	7A1
C107	CAP1	7A5
C108	CAP1	7C2
C109	CAP1	21B1
C110	CAP1	21B1
D1	LED	22B7
D2	LED	18A7
D3	LED	11A7
D4	LED	11D7
D5	LED	11C7
D6	LED	11D7
D7	LED	11B7
D8	LED	11D7
D9	LED	11B7
D10	LED	11D7
D11	LED	11B7
D12	LED	11C7
D13	LED	11B7
D14	LED	11C7
D15	LED	11B7
D16	LED	11C7
D17	LED	11A7
D18	LED	11C7
D19	LED	11A7
D20	LED	13A2
D21	SCHOTTKYDIODE1	21D4
D22	SCHOTTKYDIODE1	22D8
D23	SCHOTTKYDIODE1	22A6
H1	4_40_HDWR	22B1
H2	4_40_HDWR	22B1
H3	4_40_HDWR	22A1
H4	4_40_HDWR	22A1
J1	CONN_DB9P	16A5
J2	USB_BCON_U	16D8
J3	POWER_JACK	22D8
J4	CONN_40P	19A5
J5	CONN_BNC_5P	11D1
J6	CONN_14P	16C3
J7	CONN_BNC_5P	11A2
J8	CONN_BNC_5P	11D1
J9	CONN_14P	19D7
J10	CONN_14P	19C7
J11	CONN_14P	19D7
J12	CONN_14P	19C5
J13	CONN_14P	19D5
J14	CONN_14P	19C5
J15	CONN_14P	19D5
J16	CONN_14P	19C3
J17	CONN_14P	19D3
J18	CONN_14P	19C3
J19	CONN_14P	19D2
J20	CONN_14P	19B1
J21	CONN_14P	19D1
J22	CONN_14P	19A7
J23	CONN_14P	19B7
J24	CONN_14P	19C7
J25	CONN_14P	19B7
J26	JMP_OPEN_2P	9B4
J27	JMP_OPEN_2P	10D8
J28	CONN_BNC_5P	10D7
J29	CONN_BNC_5P	10C7
J30	CONN_BNC_5P	9A3
J31	CONN_BNC_5P	9B3
J32	JMP_OPEN_2P	9D4
J33	JMP_OPEN_2P	10B8
J34	CONN_BNC_5P	10B7
J35	CONN_BNC_5P	10A7
J36	CONN_BNC_5P	9C3
J37	CONN_BNC_5P	9D3
J38	JMP_OPEN_2P	9B8
J39	JMP_OPEN_2P	10D4
J40	CONN_BNC_5P	10D3
J41	CONN_BNC_5P	10C3
J42	CONN_BNC_5P	9A8
J43	CONN_BNC_5P	9B8
J44	JMP3	22A8
J45	JMP3	22A7
J46	JMP3	22A7
J47	JMP_OPEN_2P	9D8
J48	JMP_OPEN_2P	10B4
J49	CONN_BNC_5P	10B3
J50	CONN_BNC_5P	10A3
J51	CONN_BNC_5P	9C8
J52	CONN_BNC_5P	9D8
J53	RJ45_8	7B4 7B7 7D4 7D8
J54	RJ45_8	8B4 8B8 8D4 8D8
L1	COIL_2P	17D6
R1	RES1	12A7
R2	RES1	12B7
R3	RES1	20C4
R4	RES1	20A4
R5	RES1	20C4
R6	RES1	20A4
R7	RES1	20C2
R8	RES1	20C4
R9	RES1	20C2
R10	RES1	20C7
R11	RES1	20A4
R12	RES1	20A2
R13	RES1	20D2
R14	RES1	20B2
R15	RES1	11C4
R16	RES1	20B2
R17	RES1	20C2
R18	RES1	20D2
R19	RES1	11C4
R20	RES1	11D4
R21	RES1	20C6
R22	RES1	20B2
R23	RES1	21C5
R24	RES1	20C6
R25	RES1	20D7
R26	RES1	20D6
R27	RES1	20C2
R28	RES1	20B4
R29	RES1	20D4
R30	RES1	20B4
R31	RES1	20D7
R32	RES1	20D4
R33	RES1	20B4
R34	RES1	20B4
R35	RES1	20A2
R36	RES1	20D7
R37	RES1	17A1
R38	RES1	17A1
R39	RES1	11D5
R40	RES1	22B7
R41	RES1	16C8
R42	RES1	11C4
R43	RES1	16D7
R44	RES1	16C8
R45	RES1	16A5
R46	RES1	11B2
R47	RES1	16C1
R48	RES1	16C1
R49	RES1	16A4
R50	RES1	16A5
R51	RES1	11D2
R52	RES1	17A7
R53	RES1	11A5
R54	RES1	17A4
R55	RES1	16C3
R56	RES1	16D6
R57	RES1	17A7
R58	RES1	16B2
R59	RES1	16B1
R60	RES1	18A2
R61	RES1	12A2
R62	RES1	16C7
R63	RES1	11C2
R64	RES1	11D2
R65	RES1	17D4
R66	RES1	18B3
R67	RES1	18B6
R68	RES1	18A2
R69	RES1	18A5
R70	RES1	18A7
R71	RES1	18B2
R72	RES1	17A1
R73	RES1	11A6
R74	RES1	18B2
R75	RES1	17A2
R76	RES1	18A4
R77	RES1	11C6
R78	RES1	11D6
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R80	RES1	18B3
R81	RES1	12C5
R82	RES1	12D5
R83	RES1	11B6
R84	RES1	11D6
R85	RES1	12B7
R86	RES1	11B6
R87	RES1	11D6
R88	RES1	18B2
R89	RES1	18B3
R90	RES1	12A7
R91	RES1	18A2
R92	RES1	11B6
R93	RES1	11D6
R94	RES1	11A2
R95	RES1	11B6
R96	RES1	11C6
R97	RES1	11A6
R98	RES1	11C6
R99	RES1	11A5
R100	RES1	11A6
R101	RES1	11C6
R102	RES1	11C4
R103	RES1	11C5
R104	RES1	12A5
R105	RES1	12A6
R106	RES1	11A6
R107	RES1	11C6
R108	RES1	13A2
R109	RES1	20A4
R110	RES1	12A3
R111	RES1	9A6
R112	RES1	9C2
R113	RES1	9A6
R114	RES1	9C2

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R115	RES1	9A2
R116	RES1	20C7
R117	RES1	9A2
R118	RES1	10C6
R119	RES1	9C6
R120	RES1	20C4
R121	RES1	20C7
R122	RES1	20C7
R123	RES1	10C6
R124	RES1	9C6
R125	RES1	10A6
R126	RES1	20D6
R127	RES1	8C2
R128	RES1	10A6
R129	RES1	8C2
R130	RES1	20D2
R131	RES1	20C6
R132	RES1	20A2
R133	RES1	10C2
R134	RES1	20B2
R135	RES1	20D2
R136	RES1	20D6
R137	RES1	20C6
R138	RES1	11D5
R139	RES1	20A2
R140	RES1	20D6
R141	RES1	10C2
R142	RES1	8A2
R143	RES1	10A2
R144	RES1	8A2
R145	RES1	21D5
R146	RES1	10A2
R147	RES1	8A6
R148	RES1	20D7
R149	RES1	8A6
R150	RES1	7C6
R151	RES1	20D4
R152	RES1	7C6
R153	RES1	20D4
R154	RES1	8C6
R155	RES1	7A6
R156	RES1	7A2
R157	RES1	7C2
R158	RES1	8C6
R159	RES1	7A6
R160	RES1	7A2
R161	RES1	7C2
SW1	PUSHBUTTON	11A5
SW2	PUSHBUTTON	17A8
SW3	SWITCH_DPDT_SLIDE_6P	18A6
SW4	SWITCH_DPDT_SLIDE_6P	16C4
SW5	SWITCH_DPDT_SLIDE_6P	18A8
SW6	PUSHBUTTON	12B3
SW7	SWITCH_DPDT_SLIDE_6P	12A2
T1	XFMR_QUADT1E1_TG83_U	7A3 7A7 7B3 7B6 7C3 7C7 7D3 7D7
T2	XFMR_QUADT1E1_TG83_U	8A3 8A7 8B3 8B7 8C3 8C7 8D3 8D7
T3	XFMR_QUADT1E1_TG83_U	9A3 9A7 9B2 9B7 9C3 9C7 9D2 9D7
T4	XFMR_QUADT1E1_TG83_U	10A3 10A7 10B2 10B7 10C3 10C7 10D3 10D7
U1	FT245BM_U	16C6
U2	MMC2107_1	17C2 17C6
U3	CY62128V_2	18C7
U4	DS2174	12C7
U5	XC2S_FG256	13C6 14C5 15C5
U6	DS26334_U	2B5 3B3 3B7 3D3 3D7 4B3 4B7 4D3 4D7 5B3 5B7 5D3 5D7 6B3 6B7 6D3 6D7
U7	DS232	16A7
U8	NC7SZ86_U	11D2
U9	MAX1793_U	21D7
U10	CY62128V_2	18C3
U11	NC7SZ86_U	11D2
U12	XC18V02VQ44C	12D3
U13	74_04_U	11A7 11B7 11B8 13A3 17A6 22A2
U14	74_04_U	11C7 11C8 11D7 11D8

U15	MAX1792_1	21D3
U16	XCFS_VO20	13B2
U17	74_00	11B4 17A6 22B2
U18	74_04_U	11B7 11B8 11B8 11C7 11C7 11C8
U19	MAX6816_2	12B2
U20	MAX1793_U	21D5
X1	XTAL_U	16C7
X2	XTAL	17A4
Y1	OSC2	11B2
Y2	OSC2	11C2

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